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EXPERTISE

- ***VLSI***
- ***Analog design***

RESEARCH

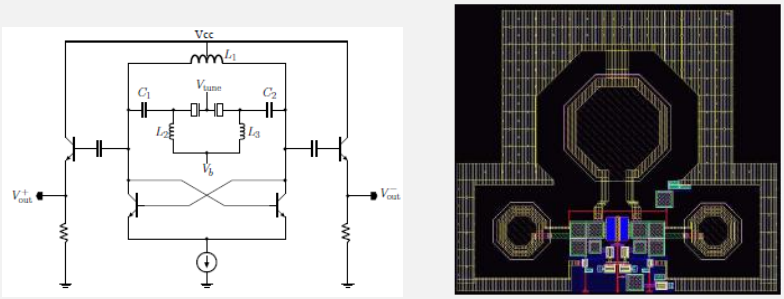
- ***Frequency synthesizer***
- ***RF transceivers***

PROFESIONAL AFFILIATIONS

- ***BEM (member)***

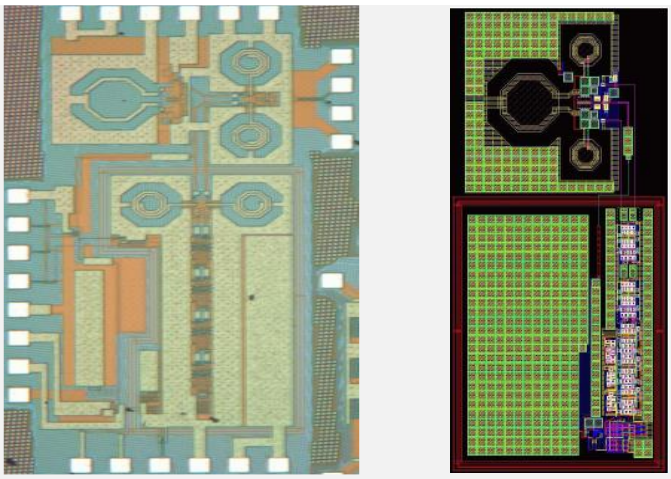
CONTACT

BRIEF RESEARCH/COMMUNITY/CONSULTATION SNAPSHOT



(a) (b)

Fig. 1 (a) VCO circuit (b) VCO layout



(a) (b)

Fig. 2. (a) PLL in the GLIMMR test chip (b) PLL layout

SELECTED PUBLICATIONS

1. ***"Review of low power digital delay locked loop (DLL)," (2015) Journal of Theoretical & Applied Information Technology 77(2) pp. 259-265.***
2. ***"A low power phase frequency detector for delay-locked loop," (2015) Journal of Theoretical & Applied Information Technology 74(3) pp. 391-397.***
3. ***"Design of a Current Starved Ring Oscillator Based VCO for Phase-Locked Loop," (2014) TELKOMNIKA Indonesian Journal of Electrical Engineering pp. 6667-6672.***
4. ***"Reference spur suppression technique using ratioed current charge pump," (2013) Electronics Letters 49(12) pp. 746-747.***
5. ***"An accurate analytical spur model for an integer-N phase-locked loop," (2012) 4th International Conference on Intelligent and Advanced Systems pp. 659-664.***

6. *"A phase-locked loop reference spur modelling using simulink," (2012) Intl. Conf. on Electronic Devices, Systems and Applications. pp. 279-283.*
7. *"A SiGe 6 modulus prescaler for a 60 GHz frequency synthesizer," (2007) Proc. SPIE, Microelectronics: Design, Technology, and Packaging III pp. 67980E-67980E-9.*