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PENAPIS PEMUAT TERSUIS UNTUK PENGUKURAN AKUSTIK

Mohd Alauddin Mohd Ali[1]

ABSTRAK

Teknik-teknik pemuat tersuis digunakan untuk merekabentuk suatu litar penuras jalur laluan yang memenuhi tentuan penuras-penuras yang diperlukan dalam pengukuran akustik. Kebersandaran ciri-ciri penuras pemuat tersuis kepada frekuensi jamnya mengizinkan pencapaian keseluruhan julat frekuensi jalur tengah yang diutamakan dari 10 Hz ke 20 kHz oleh suatu litar tunggal. Rekabentuk ini menghasilkan suatu litar yang tak peka terhadap kemuatan berparasit dan perubahan nilai unsur. Keadaan ini memungkinkan penuras tersebut dan kesemua alat tambahnya dijadikan terkamir penuh dengan menggunakan teknologi MOS.

ABSTRACT

Switched-capacitor techniques are applied to the design of a bandpass filter circuit satisfying the specification for filters used in acoustical measurement. Dependence of the switched-capacitor filter characteristics on its clock frequency allows the achievement of the whole range of preferred midband frequencies from 10 Hz to 20 kHz by a single circuit. The design produces a circuit which is insensitive to parasitic capacitances and element-value variations. This offers the possibility for the filter and all its accessories to be fully integrated using MOS technology.

INTRODUCTION

Switched-capacitor (SC) techniques and metal-oxide-semiconductor (MOS) technology offer the possibility of implementing precise fully integrated high quality filters (Brodersen, Gray, and Hodges 1979). The Switched-capacitor filters (SCF), as they are called, consist only of capacitors, operational amplifiers (OA) and analogue switches which are all easily implemented in MOS integrated circuit (IC). The filter parameters are determined by the capacitor ratios and the frequency at which the switches are clocked. Using MOS technology, accurate capacitor ratios, which are relatively insensitive to drift, are realisable within a small silicon area.

In this paper, we report the application of SC techniques to the design of bandpass filters used in the analysis of acoustic noise and vibration. Active-RC filters have previously been designed for this purpose meeting specifications such as given by the British Standard 2475:1964. In these filters, however, filter parameters are dependent on the absolute values of resistors and capacitors. These values are difficult to control in current IC technology, thus active-RC filters are not suitable for precise integrated implementation. Furthermore, a set of these filters are required to provide for the various preferred midband frequencies in the specification.

The SC techniques overcome the above problems and simplify the filter implementation. All the filter characteristics with different midband frequencies can be obtained from a single circuit by only varying the clock frequency of the filter. The following sections show how this circuit is derived considering the design constraints posed by current IC technology.

FILTER REQUIREMENTS

The British Standard 2475:1964 gives specification for one-third octave bandpass (OTOB) filters which is shown in Figure 1. The critical frequencies in the Figure are given in terms of the midband frequency, f_m as follows:

$$f_{+i} = 2^{i/24} f_m \qquad \text{for } i = 1,2,3$$

$$= 2^{i-2} f_m \qquad \text{for } i = 4,5$$

and (1)

$$f_{-i} = f_m^2 / f_{+i}$$

A set of filters with the above specification is required for acoustic noise measurement. The preferred values for f_m are given by

$$f_m = 1000 \times 10^{i/10}$$

for all integer i, (2)

$$-20 < i < 13$$

In other words, the lowest f_m required is 10 Hz and the highest is 20 kHz.

The specification in Figure. 1 can be satisfied by a fourth order Butterworth bandpass filter which can be realised by the doubly-terminated LC ladder network shown in Figure. 2. Normalised values of the components are

$$R_T = 1\Omega,\ L_A = 1.1306H,\ L_B = 0.0224H$$

$$C_B = 1.1306F,\ C_A = 0.0224F \qquad (3)$$

DERIVATION OF THE SCF

Design Method

A number of methods have been proposed for the design of SCF (Gregorian, Martin, and Temes, 1983). Among these, the design of high order SCF by simulating the doubly-terminated LC ladder network is the most attractive due to its low sensitivity to element-value variations (Inoue and Ueno, 1987). This method itself leads to a number of design approaches. The signal flow graph (SFG) design strategy using SC integrators (SCI) is here chosen.

This design method starts by transforming the differential equations describing the passive ladder network into an SFG. This graph is manipulated in order to obtain a representation which can be realised by using integrators. A complete set of loop and node equations for the ladder network in Figure. 2 which involves only integrators is given below.

$$
\begin{aligned}
V_3 &= V_{IN} - V_1 - V_2 - V_4 \\
V_1 &= I_1 R_T \\
V_2 &= I_1 / sC_A \\
V_4 &= I_2 / sC_B \\
I_1 &= V_3 / sL_A \\
I_3 &= V_4 / sL_B \\
I_4 &= V_4 / R_T \\
I_2 &= I_1 - I_3 - I_4
\end{aligned}
\qquad (4)
$$

An SFG representing these equations is given in Figure. 3. It shows that four integrators are required with two of them damped to incorporate the terminations of the ladder network.

In active-RC network these are realised by continuous-time integrators as shown in Figure. 4. The integrator in Figure. 4(a) has the transfer function

$$H(s) = - \frac{1}{R_1 C_2 s} \tag{5}$$

whereas for the damped integrator in Figure. 4(b), it is

$$H(s) = - \frac{1/R_1 C_2}{s + 1/R_3 C_2} \tag{6}$$

Constants in these transfer functions are dependent on the resistor and capacitor values.

Switched–capacitor integrators

The SCF is derived from the SFG by using SCI. Figure 5 shows an inverting SCI where each switching component represents two MOS field-effect transistors (MOSFET) as in Figure 6(a) (Martin, 1980). They are controlled by a two-phase non-overlapping clock with frequency, $f_c = 1/T$ as shown in Figure 6(b). With this timing scheme, the z-transform transfer function of the SCI is (Laker, 1979)

$$H^{eo} = - \frac{C_1}{C_2} \frac{z^{-1/2}}{1-z^{-1}} \tag{7}$$

where H^{eo} means that the input and output are sampled during the even, ϕ_e and odd, ϕ_o clock phases respectively. Figure 7 shows a non-inverting SCI which realises the transfer function in (7) without the negative sign (Martin, 1980).

Comparison of equations (5) and (7) shows that the SCI is actually an implementation of the continuous-time integrator through the Lossless Discrete Integrator (LDI) transformation (Bruton, 1975)

$$s \rightarrow \frac{1}{T} \frac{1-z^{-1}}{z^{-1/2}} \tag{8}$$

The resistor value is replaced by the switched-capacitor value according to

$$R_1 = T/C_1 \tag{9}$$

The integrator gain constant in this case is dependent on a capacitor ratio and the clock frequency. This is further clarified by evaluating the frequency response of the SCI by setting $z = \exp(j\omega T)$ in (7) to obtain

$$H(\omega) = -\frac{f_c C_1}{C_2} \cdot \frac{1}{j\omega} \cdot \frac{\omega T/2}{\sin(\omega T/2)} \tag{10}$$

The response in (10) is similar to that of a continuous-time integrator except for the deviation term given in the bracket. This deviation can be neglected if f_c is large compared to the signal frequencies (i.e. $\omega T << 1$). Otherwise the deviation can be adjusted, according to the LDI transformation, by prewarping the continuous-time frequency, Ω using

$$\Omega = \frac{2}{T} \sin(\omega T/2) \tag{11}$$

The advantage of the SCI circuits associated with the LDI transformation is that they are completely insensitive to stray capacitances between any node and ground. Hence they can be practically implemented on chip using very small capacitance values. However, a problem arises when the damped integrator is to be implemented through the LDI transformation. Applying (8) and (9) to equation (6), the transfer function becomes

$$H(z) = -\frac{(C_1/C_2)\, z^{-1/2}}{1 + (C_3/C_2) z^{-1/2} - z^{-1}} \tag{12}$$

The $z^{-1/2}$ term in the denominator associated with the damping resistor R_3 is not realisable by SC circuits (Davis and Trick, 1980). Thus the termination in ladder networks cannot be realised exactly through the LDI transformation.

The $z^{-1/2}$ term can, however, be approximated by $(1+z^{-1})/2$ (Lee and Chang, 1980). Error associated with this approximation is purely real affecting only the element values with no dissipative effect and hence causing very small distortion in the frequency response. This error can be neglected altogether if $\omega T << 1$. Using this approximation, equation (12) becomes

$$H^{eo} = - \frac{(C_1/C_2)\, z^{-1/2}}{1 + C_3/2C_2 - [1 - (C_3/2C_2)]z^{-1}} \qquad (13)$$

This transfer function can be realised by the damped SCI in Figure 8 which is also parasitic-insensitive (Martin, 1980). The ratios of the input SC and the feedback SC to the integrating capacitor are given by

$$K_I = \frac{C_I/C_2}{1 - C_3/2C_2} \quad , \qquad I = 1,3 \qquad (14)$$

where C_1 and C_3 are related, as in equation (9), to resistors of the damped integrator in Figure 4(b), R_1 and R_3 respectively.

Filter Circuit

Using the SCI circuits in Figures 6, 7 and 8, the SCF can be derived from the SFG in Figure. 3 and is shown in Figure 9. By comparing the SCF to the SFG and referring to equations (5), (9) and (14), the capacitor ratios for the SCF can be obtained in terms of the passive ladder component values. With $R_T = 1\Omega$, they are

$$K_0 = K_1 = K_3 = K_4 = K_6 = \frac{T/L_A}{1 - T/2L_A}$$

$$K_2 = K_5 = T/C_A \qquad (15)$$

It is also desirable for the SC realisation of the ladder network to be scaled for maximum dynamic range. This is done by analysing the passive circuit to determine the maxima of the relevant voltages and currents. These maxima are then used to scale the capacitor ratios such that the maximum output of the OAs in the SC circuits are all equal for a constant-amplitude swept frequency input (Martin and Sedra, 1978).

In the SC realisation of the passive ladder in Figure. 2, the OA outputs simulate I_1, V_2, I_3 and V_4. The maxima of these variables are obtained by analysing the ladder network using a constant amplitude input of 1V and they respectively have values

$$M_1 = 0.636A \ , \ M_2 = 4.899V$$

$$M_3 = 3.651A \ , \ M_4 = 0.500V \qquad (16)$$

In scaling the capacitor ratios using these maxima, it can be observed from Figure. 9 that for K_1C, two different capacitors are required to scale the OA outputs V_2 and V_4. Similarly, two different capacitors are required for K_4C.

The SC implementation of the passive ladder with optimum dynamic range is given in Figure. 10 where switch sharing is also implemented to reduce the number of switches. As an example, in Figure. 9, capacitors K_1C and K_3C are simultaneously switched to the input of the OA, thus they can share a common switching component. The expressions for the scaled capacitor ratios are:

$$K_1 = (M_2/M_1)K_3 \quad , \ K_1' = (M_4/M_1)K_3$$

$$K_4 = (M_3/M_4)K_6 \quad , \ K_4' = (M_1/M_4)K_6 \qquad (17)$$

$$K_4 = (M_1/M_2)(T/C_A) \quad . K_5 = (M_4/M_3)(T/C_A)$$

$$K_0 = K_3/M_1$$

where K_3 and K_6 are the same as in (15).

FURTHER DESIGN CONSIDERATIONS

In arriving to the circuit of Figure. 10, sensitivities to element-value variations and parasitic capacitances have been considered. The circuit requires only two clock phases and four OAs which allow simple and practical implementation on chip. A few more considerations, which will determine the choice for the clock frequency, are given below.

Component non-idealities

Non-ideal switches and OAs are causes of deviation in the behaviour of SCFs. Their effects, however, are mainly frequency dependent. A range of frequencies can thus be found where the effects of these non-idealities are negligible. Leakage in MOS transistor switch during its off-state limits the use of low f_c to a few hundred Hertz. The leakage currents appear as a component of the SCF output voltage offset.

The switch on-resistance and finite OA unity gain-bandwidth, on the other hand, have effects on the maximum allowable f_c. The OA slow rate and settling time are other factors which limit the use of very high f_c. To date, f_c of 18MHz has been possible (Tawfik and Senn, 1987).

Noise Considerations

Noise is another limiting factor in the use of the SCF. The important sources of noise are the thermal noise in the MOS transistor switches, the wideband thermal noise and the 1/f noise of the OA (Bordersen, Gray, and Hodges 1979). The thermal noise of the switches, or referred to as the kT/C noise, limits the use of very small capacitors on chip.

The 1/f noise, which is dominant in low frequency applications, and the wideband noise can be reduced through transistor channel modification or certain circuit techniques. However, a dynamic range of up to 90 dB is still possible without these modifications. Thus, they are not necessary in this case.

Capacitance Spread

The spread of the capacitor values will affect the accuracy of capacitor ratio definition in monolithic implementation. Large capacitance spread also means large capacitors have to be implemented on chip. Besides requiring larger chip area, this will also affect the OA settling time. The spread will increase with f_c as shown by equation (10). Designing the filter for optimum dynamic range also leads to large capacitor ratios as evident in (16) and (17). Since optimum dynamic range is desirable, in this case, the capacitance spread has to be optimised by the choice of f_c.

Antialiasing Requirement

The SCF, being a sampled-data network, requires an antialiasing filter (AAF) to bandlimit its input signal. To avoid any external components, the continuous-time AAF has also to be realised on the same chip with the SCF. The Sallen and Key section, designed to have a second-order Butterworth lowpass response, is usually used. The absolute value of resistance implemented on chip has large variation though the ratio of two resistors will generally track very closely. Thus the quality factor of the pole pair of the AAF remains constant while its cut-off frequency, f_o varies with the resistance absolute value.

The variation of f_o of the AAF filter imposes requirement for a higher f_c on the SCF. In order not to cause much drop in the SCF responce, the nominal f_o has to be chosen quite high as compared to f_m. This will require f_c to be much higher so that the AAF has 60 dB attenuation at f_c-f_m as required by the specification. Furthermore, the f_m is variable between 10Hz and 20 kHz. Thus it is required that the AAF has enough attenuation at f_c for the 10 Hz filter while not affecting the 20 kHz filter. Hence the required f_c becomes extremely large as compared to f_m.

A novel solution to this problem is through the use of the SC Decimator circuit proposed by von Grunigen, *et al* (1982). The circuit, clocked at nf_c, suppresses response around f_c and its multiples except at the multiples of nf_c. Thus a lower f_c can be chosen while the AAF now needs to have 60 dB attenuation at nf_c-f_m. The integer n can

take different values to account for the variability of f_m. Its choice is only limited by the allowable capacitance spread since it determines the ratio of capacitors in the decimator circuit. The different n values can be incorporated in a single SC Decimator circuit by using programmable SC arrays (Allstot, Brodersen, and Gray 1979).

EXPERIMENTAL FILTER

Based on the above considerations, $f_c = 48\ f_m$ was chosen for the SCF. With such f_c, prewarping is not necessary in the design. Thus the capacitor ratios can be calculated directly from equations (3), (16) and (17). The circuit in Figure. 10 is implemented using discrete analogue switches, operational amplifiers and capacitors. The capacitors were chosen to within ± 1% of their design values. Capacitor values in the 100 pF to 10 nF range were used. These are actually more than a hundred times the capacitance level when implemented on chip.

Figure. 11 gives the gain response of the SC OTOB filter implemented as above with f_c = 48 kHz. Figure. 12 gives the passband on an expanded frequency scale. These Figure show that the specification is met satisfactorily with f_m = 1 kHz achieved. Satisfactory results were also obtained for lower clock frequencies with similar performance achieved even for f_m = 10 Hz. For f_c above 60 kHz, the capacitance level chosen above has to be lowered for the circuit to be satisfactory.

CONCLUSION

A single bandpass SCF circuit has been shown to be suitable for meeting the requirements of filters for noise measurement and vibrational analysis. Midband frequencies in the range of 10 Hz to 20 kHz or more can be obtained by only varying the clock frequency of the circuit. The designed circuit gives allowance for simple and practical monolithic implementation. This possibility offers the means for implementing the filter, circuits meeting its antialiasing requirements, digital control circuits for varying the clock frequency and all other accessories on a single chip.

NOTATION

C	capacitance
C_i	capacitances of the integrator circuits
C_A, C_B	normalised capacitance values of the passive laddernetwork (PLN)
f	frequency in Hz
f_c	clock frequency of the SCF
f_m	midband frequency of the SCF
f_o	cut-off frequency of the AAF
f_{+i}, f_{-i}	critical frequencies in the SCF specification
$H(s)$	voltage transfer function of a network
$H(w)$	frequency response of a network
$H(z)$	z-domain transfer function of a network
H^{eo}	H(z) of a network with its input and output sampled during the even and odd clock phases respectively
i	integer
I_i	currents in the PLN
k	Boltzmann's constant
K_i, K_i'	capacitor ratios of the SCF
L_A, L_B	normalised inductance values of the PLN
M_i	maxima of the OA outputs
n	multiples of the clock frequency
R_i	resistances of the continuous-time integrators
R_T	terminating resistance of the PLN
s	generalised frequency variable

T	clock period, $T = 1/f_c$
T	temperature in Kelvin
V_i	voltages in the PLN
V_{IN}	input voltage to the filters
V_{OUT}	output voltage of the filters
w	discrete-time frequencies in rad/sec
z	transformed variable defined as $z = \exp(sT)$
Ω	continuous-time frequencies in rad/sec
ϕ_e, ϕ_o	even, odd phases of the clock waveform

ABBREVIATION

AAF	antialiasing filter
IC	integrated circuit
LC	inductor-capacitor
LDI	lossless discrete integrator
MOS	metal-oxide semiconductor
MOSFET	MOS field-effect transistor
OA	operational amplifier
OTOB	one-third octave bandpass
PLN	passive ladder network
RC	resistor-capacitor
SC	switched-capacitor
SCF	switched-capacitor filter
SCI	switched-capacitor integrator
SFG	signal flow graph

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1 Jabatan Kejuruteraan Elektrik, Elektronik & Sistem
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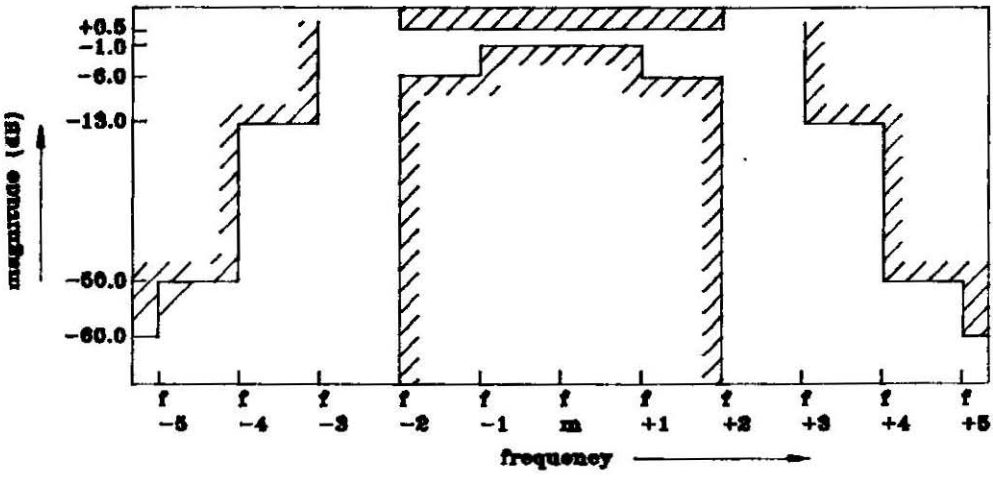

Figure 1

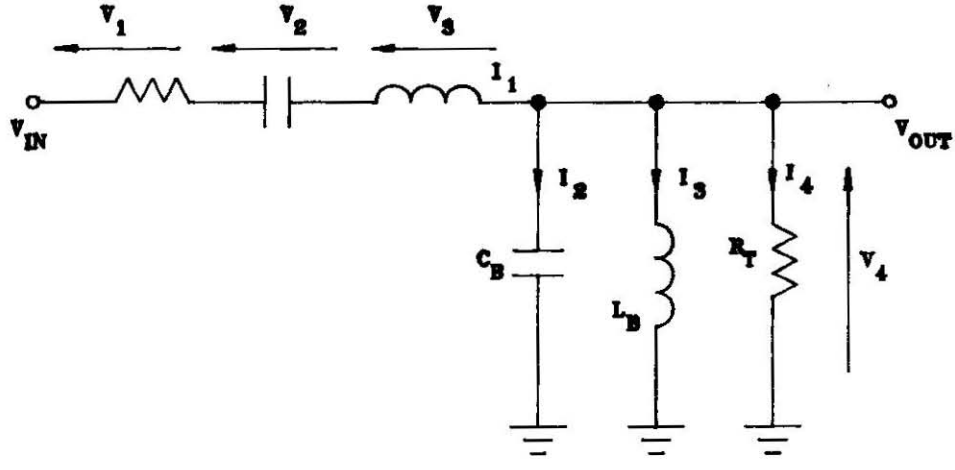

Figure 2

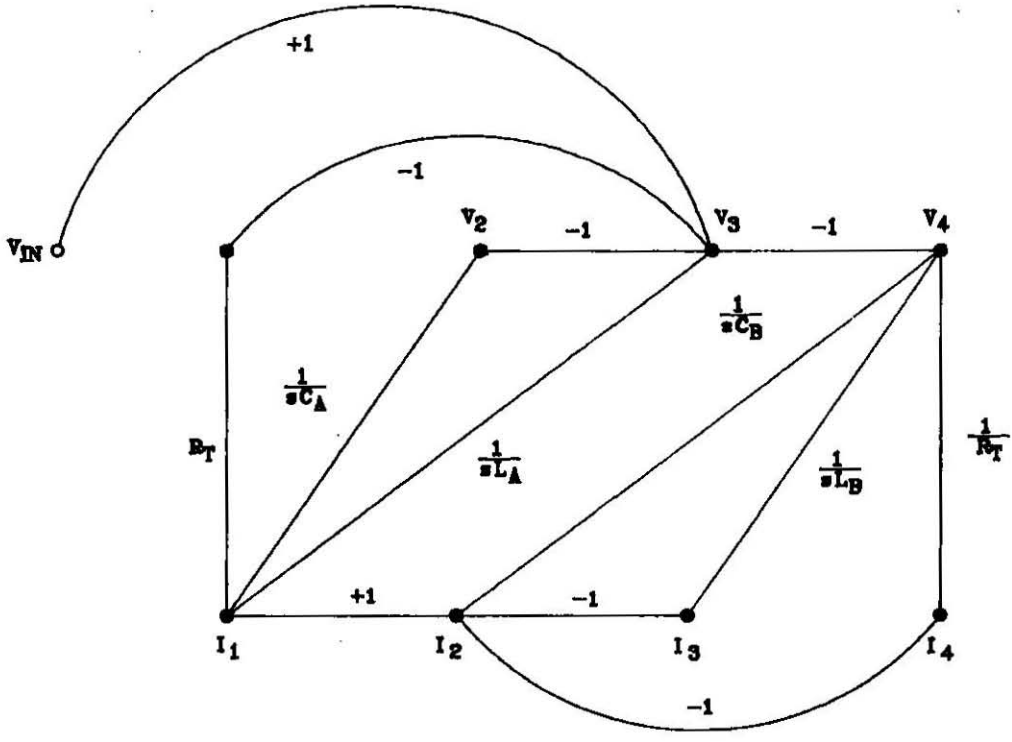
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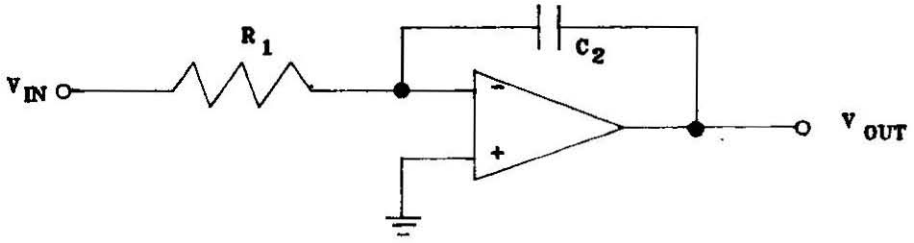
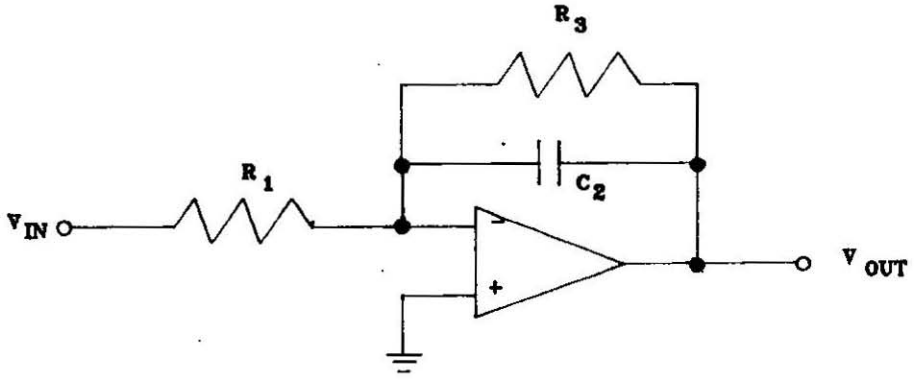
Figure 3



(a)



(b)

Figure 4

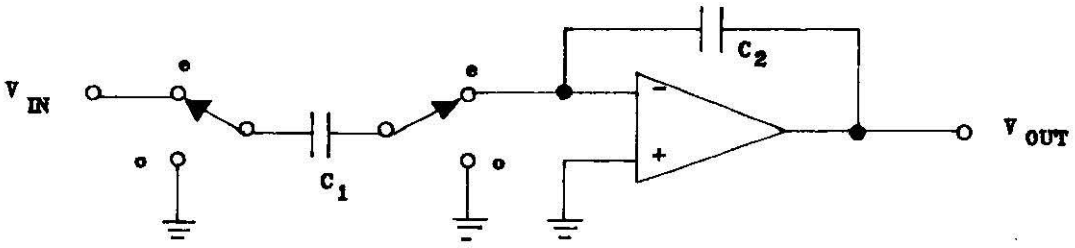
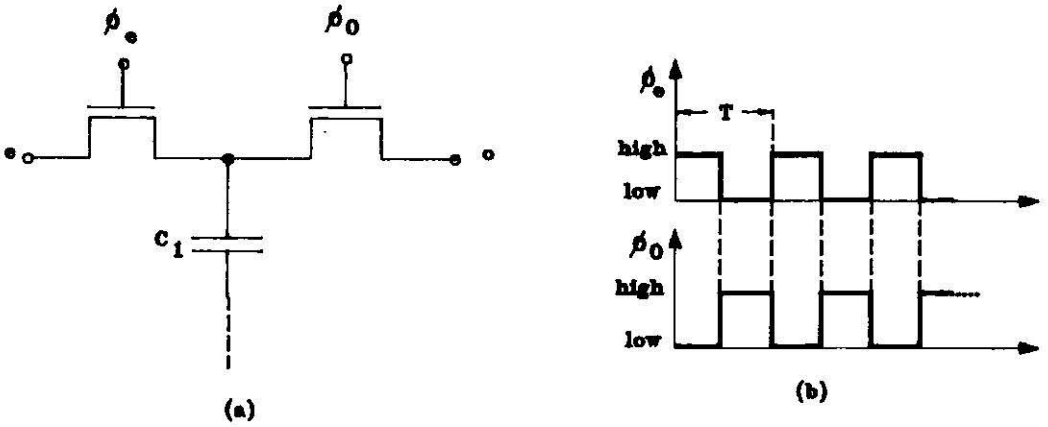


Figure 5



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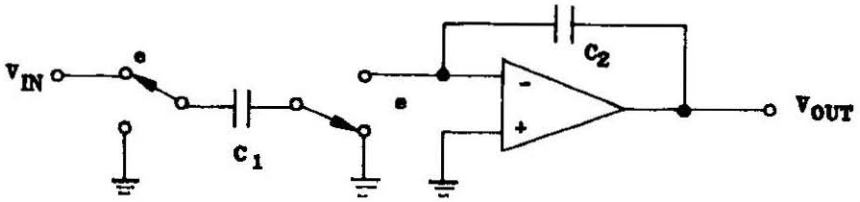

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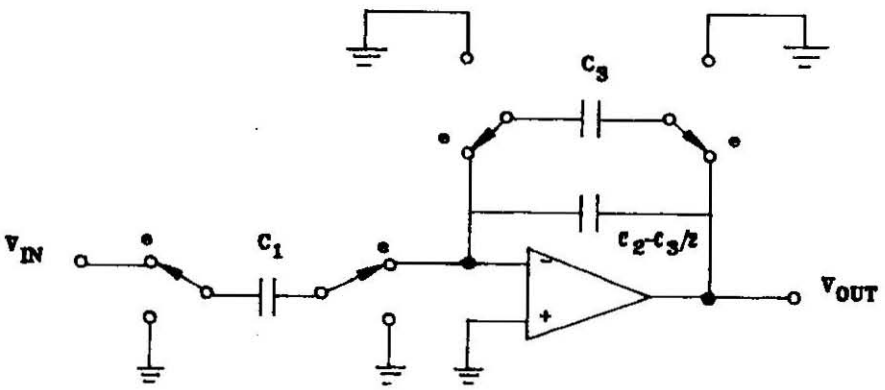

Figure 8

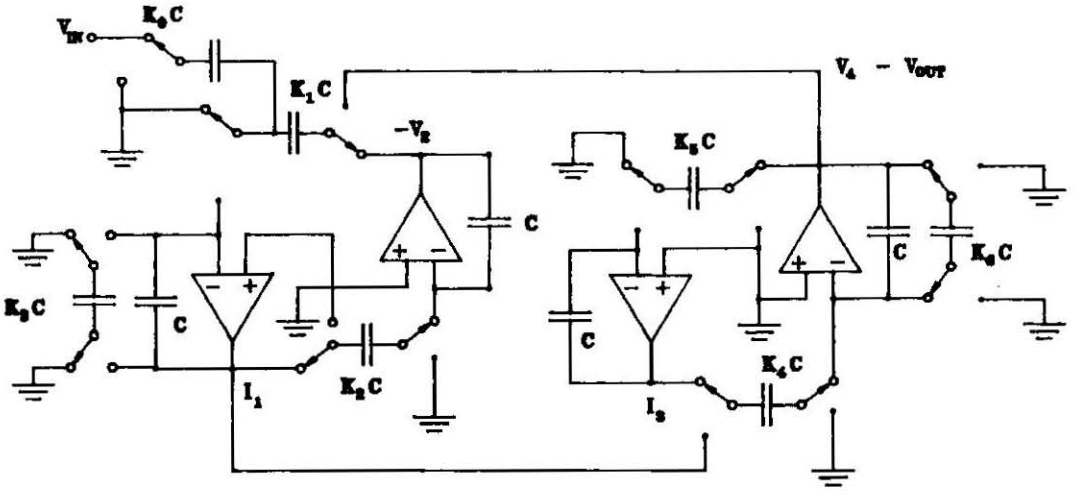

Figure 9

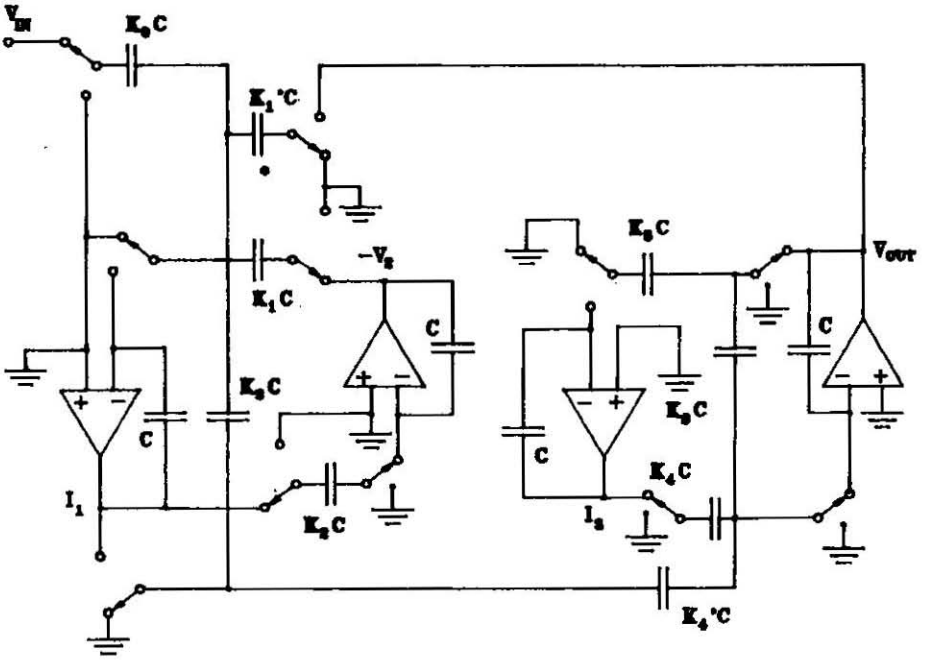

Figure 10

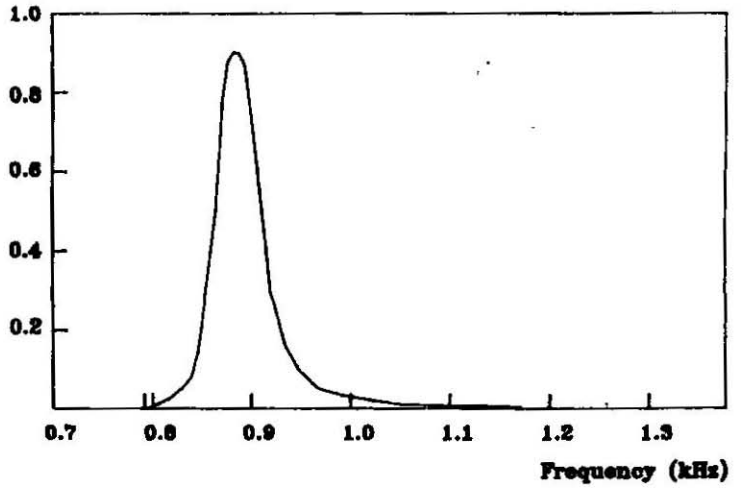

Figure 11

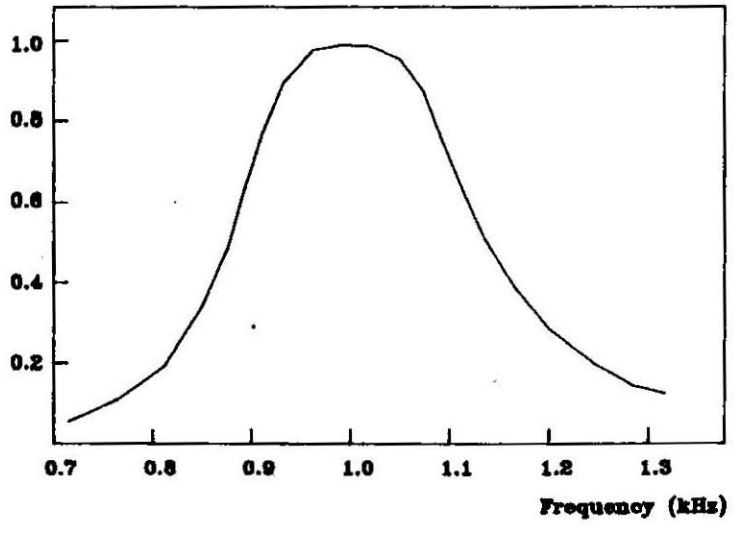

Figure 12