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A Method of Realizing XOR/XNOR Gate using Symmetric Boolean Function Lattice Structure

(Suatu Kaedah Merealisasikan Get XOR/XNOR menggunakan Struktur Kekisi Fungsi Boolean Simetri)

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ABSTRACT

The current CMOS's industry standard XOR and XNOR gate consist of 12 and 10 transistors, respectively. This transistor count could be lowered down to produce low power circuits as XOR/XNOR are extensively used in many functional modules. As a solution, a method for realizing low transistor count XOR/XNOR gates using a special property of symmetric Boolean function is proposed. This property suggests that the circuits for such functions can be realized with fewer transistors using a special lattice structure circuit. Modifications are made to the original lattice structure to match with the current CMOS technology requirements. The final circuits require eight transistors each for XOR/XNOR with mixtures of NMOS and PMOS at push-up and pull-down networks. Simulations show that the intended logic functions of XOR/XNOR are achieved. The reading of actual voltage swing, however, shows that the output is either 0.3 V over ground or below VDD when there is a mixture of NMOS and PMOS as pull-down or push-up networks, respectively. More voltage loss of 0.4 V is observed if only NMOS is at push-up or only PMOS is at pull-down networks. As a preliminary work, this achievement of the functional logic level warrants more future work to improve the loss in output voltage swing.

Keywords: XOR; XNOR; symmetric Boolean function; pass-transistor logic; CMOS; lattice structure

ABSTRAK

Ketika ini piawai industri CMOS mempunyai 12 dan 10 transistor masing-masing bagi gerbang XOR dan XNOR. Bilangan transistor ini boleh dikurangkan lagi untuk menghasilkan litar kuasa rendah kerana XOR/XNOR banyak digunakan dalam banyak modul fungsian. Sebagai satu penyelesaian untuk ini, suatu kaedah untuk merealisasikan get XOR/XNOR menggunakan ciri istimewa fungsi Boolean simetri dicadangkan. Ciri berkenaan mencadangkan bahawa litar untuk fungsi-fungsi sebegini boleh direalisasikan menggunakan bilangan transistor yang lebih rendah menggunakan litar istimewa bernama struktur kekisi. Pengubahsuaian dilakukan kepada struktur kekisi asal untuk dipadankan dengan keperluan teknologi CMOS semasa. Litar akhirnya memerlukan lapan transistor setiap satu untuk XOR/XNOR dengan campuran NMOS dan PMOS pada rangkaian tolak-naik dan tarik-turunnya. Simulasi menunjukkan bahawa fungsi XOR/XNOR yang dikehendaki telah dicapai. Bacaan julat ayunan voltan sebenar, walau bagaimanapun, telah menunjukkan bahawa keluaran adalah sama ada 0.3 V di atas bumi atau di bawah VDD apabila terdapat campuran NMOS dan PMOS dalam rangkaian tarik-turun dan dan tolak-naik masing-masing. Kehilangan voltan yang lebih tinggi, bernilai 0.4 V, diperhatikan jika hanya NMOS berada dalam rangkaian tolak-naik atau hanya PMOS berada dalam rangkaian tarik-turun. Sebagai hasil kerja awal, pencapaian paras logik fungsian ini akan membolehkan kerja-kerja baru pada masa akan datang diteruskan untuk memperbaiki kehilangan julat ayunan voltan keluaran.

Kata kunci: Pemandu; XOR; XNOR; fungsi Boolean simetri; logik laluan-transistor; CMOS; struktur kekisi

INTRODUCTION

Current computing systems are focusing more and more on low power circuits as the demand for systems on handheld devices keeps increasing. These devices run on battery power; hence power usage is of critical concern.

Lowering down power while keeping VDD constant means the current has to be lowered down. For ICs, having smaller channel size will lower down the amount of flowing current hence making the whole system running at low power. Due to this fact, until the first decade of 21st century, most of the work to improve ICs in terms of density, speed, and power was conducted by reducing the size of transistors' channel (Geiger et al. 1989).

By the second decade, the channel size of the transistors was approaching nanometer scale where the physics of microelectronics are no longer applied (Cao 2011). At the same time, more and more work to reduce transistor count were published with the aim to reduce current and power, especially in XOR/XNOR (Shoba & Nakkeeran 2016).

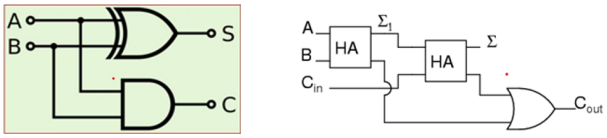
2-input XOR gate is a logic gate that gives logic 1 when it's two inputs are *different*; otherwise 0. Its inversion is XNOR gate that gives logic 1 when the two inputs are the *same*; 0 otherwise. The two truth tables are summarized in Table 1.

TABLE 1. Truth tables for XOR ($\oplus$) and XNOR ($\odot$)

A	B	A$\oplus$B	A$\odot$B	No. 1s in variable
0	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	1	2

The main reason why a lot of the work to reduce the number of transistors in ICs was conducted on XOR/XNOR is because they are the main component in realizing half adder and full adder (Kumar & Rakesh 2020; Qaleh-Jooq et al. 2020). Since adders are the main components for building almost all other functional modules like multiplier, counter, etc. including more advanced module like Booth multipliers, carry select adder (Anis-Shahida et al. 2018; Arulkarthic & Rathinaswamy 2020; Hossain & Abedin 2019), improving XOR/XNOR gate will eventually improve the whole system.

Figure 1 shows the standard circuits for half adder and full adder (consists of two half adders) respectively, to highlight the use of XOR gates in them.



(a) Half adder (b) Full adder from half adder

FIGURE 1. Half adder and full adder

SYMMETRIC BOOLEAN FUNCTIONS

XOR/XNOR fall into a class of functions called symmetric Boolean functions. Since a property of symmetric functions is used in this design, some information about symmetric Boolean functions is included in this paper. This class of function is used because it can be implemented using a special kind of circuit, called lattice structure, that uses less transistors than the conventional circuit. This is explained more in Subsection 1.2.

Symmetric Boolean function is a special class of Boolean functions that are invariant of input permutations. For a 2-input (2-variabled) function this means, F(*a,b*)=F(*b,a*). This can be extended to more variables with all possible permutations: F(*a, b, c*) = F(*a, c, b*) = F(*b, a, c*) = F(*b, c, a*) = F(*c, a, b*) = F(*c, b, a*). One can tell if the function is invariant by looking at the output column in the function's truth table. If the output column does not change by swapping the input columns, then the function is symmetric. An example of symmetric 2-input Boolean function is F(*a,b*)=ab. The two possible truth tables of F=*ab* with swapped input columns are shown in Table 2. It can be seen that the output columns (shaded) are identical.

TABLE 2. Two possible truth tables for ab - a symmetric function

a	b	ab
0	0	0
0	1	0
1	0	0
1	1	1

b	a	ab
0	0	0
0	1	0
1	0	0
1	1	1

On the other hand, one example of non-symmetric Boolean function is F(*a,b*)=a$\bar{b}$. The two truth tables in Table 3 show that the output columns changed if the input columns are swapped – second row swapped with third row.

TABLE 3. Two possible truth tables for a$\bar{b}$- a non-symmetric function

a	b	a$\bar{b}$
0	0	0
0	1	0
1	0	1
1	1	0

b	a	a$\bar{b}$
0	0	0
0	1	1
1	0	0
1	1	0

For 2-input Boolean functions there are only 16 unique functions, 8 out of which are symmetric (Muhazam 2004). Table 4 shows the complete list of them.

TABLE 4. Complete list of 16 2-Input Boolean functions and their dymmetries

a	b	F= $\overline{a+b}$ NOR symmetric	F=a$\bar{}$b b but not a non-symmetric	F=a$\bar{}$ Not a non-symmetric	F=a$\bar{}$ Not a non-symmetric
0	0	0	1	0	1
0	1	0	0	1	1
1	0	0	0	0	0
1	1	0	0	0	0

a	b	F=a$\bar{b}$ a but not b non-symmetric	F=$\bar{b}$ Not b non-symmetric	F=a$\oplus$b XOR symmetric	F= $\overline{ab}$ NAND symmetric
0	0	0	1	0	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	0	0	0	0

a	b	F=ab AND symmetric	F=a$\odot$b XNOR symmetric	F=b pass b non-symmetric	F=a$\bar{}$+b *b* or Not *a non-symmetric*
0	0	0	1	0	1
0	1	0	0	1	1
1	0	0	0	0	0
1	1	1	1	1	1

a	b	F=a pass *a non-symmetric*	F=a+ $\bar{b}$ *a* or Not *b non-symmetric*	F=a+b OR *symmetric*	F=1 constant 1 *symmetric*
0	0	0	1	0	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	1

LATTICE STRUCTURE

Lattice structure is a special self-repeating circuit pattern that can be used to implement symmetric Boolean functions (Harisson 1965). For a 2-variable symmetric Boolean function, the base VDD-seeking (positive logic) lattice structure is as shown in Figure 2.

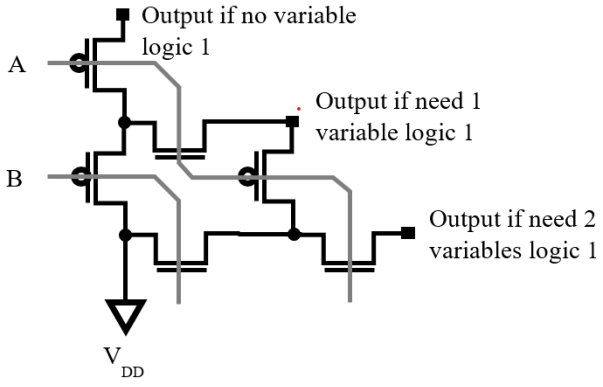


FIGURE 2. 2-variable symmetric Boolean function base

LATTICE STRUCTURE

Lattice structure circuit can also be ground-seeking (negative logic), but for this paper only the VDD-seeking will be discussed. The differences are rather trivial and self-exploratory.

The output points of the lattice structure will be selected, and combined if needed, to implement a specific symmetric function.

This circuit however, was built more on mathematical concept, not so much on real implementation. It assumes if the output points can find its way to VDD due to the switching conditions of the NMOSs and PMOSs, the output will be set to logic 1. Otherwise, it will be pulled down to ground by a pull-down network. The structure assumes the actual circuit can provide such pull-down and/or push-up networks.

RELATED WORKS

One of the best alternative technologies that could be used to fabricate ICs other than the most popular CMOS technology is the pass-transistor logic (PTL) technology. This technology differs from the conventional CMOS technology in a few aspects such as

1. There exists at least 1 transistor that is powered-up by the circuit's input signal, instead of VDD.
2. The input lines can be the power lines or the ground lines for at least 1 of the transistors.
3. There will be current drawn from the input lines.

The above properties of PTL circuits violates CMOS circuit rules since in CMOS the input signals are only allowed to control the voltage at the gates of the transistors and not to be connected to other terminals. Since the gates are electrically insulated from the transistors' channel, there is theoretically no current flowing from the input lines into the CMOS system. Nonetheless PTL has been proven to be able to produce circuits with fewer transistors.

PTL technology has a few proposed layouts for building XOR/XNOR gates (Kumar & Rakesh 2020; Geetha-Priya & Baskaran 2013; Ravali et al. 2017). Due to space constraint, only the best proposed XOR/XNOR in PTL technology will be discussed in this paper using the one proposed by Chowdhury et al. with only three transistors (Kumar & Rakesh, 2020). The schematic of the proposed XOR gate is shown in Figure 3.

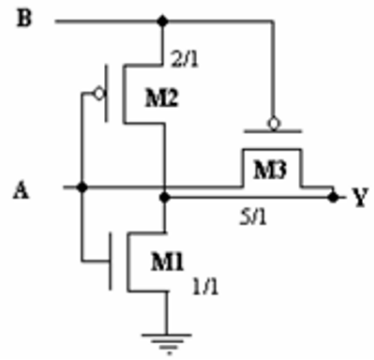


FIGURE 3. 3-transistor PTL XOR gate

The XOR behavior of the circuit can be explained as follows:

1. In an XOR gate, if one of the inputs, let's say A, is 0, the output will follow the logic of the other input, let's say B. When A is 0 in Figure 3, both transistors M1 and M2 will be turned off because input A is the one that powers up both of them. At the same time, logic 0 of A will give a conducting voltage (switch on) to the PMOS M3. If input B is logic 1, it will power up M3, then the output will get logic 1, otherwise it will transfer the logic 0 from B to output.
2. Again, in an XOR gate, if one of the inputs, let's say A, is 1, the output will get the inversion of the other input, let's say B. When A is 1 in Figure 3, it will power up M1 and M2 whose arrangement will become an inverter of the input B to the output. At the same time the high logic of A will give a non-conducting voltage (switch off) to the PMOS M3. This will block the direct signal from B hence the output will only receive the inverted signal of B.

The work on PTL technology is included in this paper to give some idea on how rigorous the research on reducing the number of transistors in XOR/XNOR had been conducted.

Other than PTL, there are also attempts in domino MOS technology (Hajiqasemi & Beitollahi 2020), analogue current mirror topology techniques (Fábio et al. 2016) and also with different types of MOS dimension – like FinFET (Bellizia et al. 2018) – to produce better XOR/XNOR. However, these optimizations are not without cost. Reducing transistor count, while lowering down current flow, it may for example lower down speed as well (Mewada et al. 2019).

PROPOSED DESIGN

STEP 1: FORMING LATTICE STRUCTURE CIRCUITS FOR XOR AND XNOR FUNCTIONS

Referring to Table 1, to output logic 1, XOR function only needs one variable to be at logic 1 – either A or B, but not both. In this case, only the middle output point from the base lattice will be taken, making the top-most PMOS and the right-most NMOS to be redundant and can be removed. This reduces the lattice structure to the layout as shown in Figure 4.

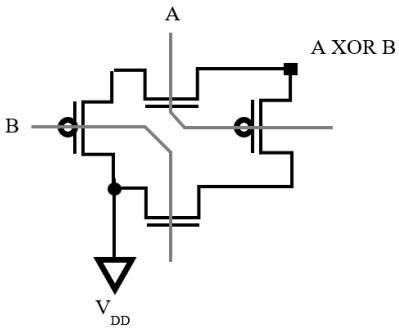


FIGURE 4. XOR function optimized lattice structure

This circuit is basically a parallel connection of two alternate series connections a PMOS and an NMOS.

The work of the lattice can be explained as follows. If A and B have the same logic state, both parallel connections will have open circuit at either PMOS or NMOS. But if A is 1 and B is 0, the path consisting of top NMOS and left hand side PMOS will connect the output to VDD, while the path of right hand side PMOS and bottom NMOS will be both open circuits. If A is 0 and B is 1, the path consisting of bottom NMOS and right hand side PMOS will connect the output to VDD, while the path of left hand side PMOS and top NMOS will be both open circuits. Either way, the output will reach VDD to get logic 1. Hence, XOR function is achieved.

Again referring to Table 1, to output logic 1, XNOR function needs either two variables (both) to be at logic 1 or none of them. In this case, the top output point and the bottom output point from the base lattice will be taken and combined, making the middle PMOS and NMOS to be redundant and can be removed. This reduces the lattice structure to the layout as shown in Figure 5.

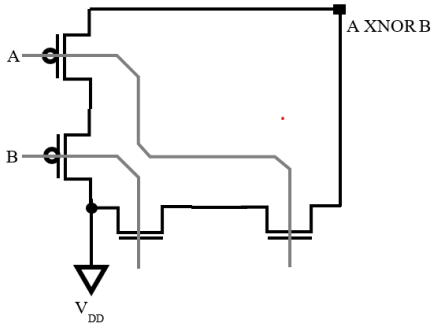


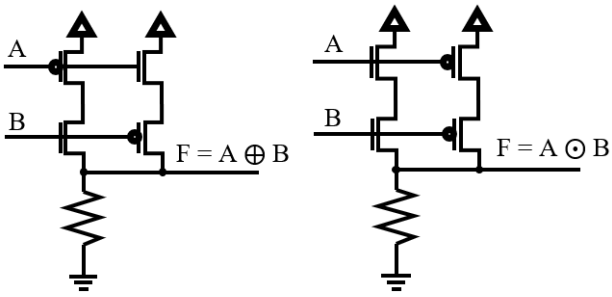
FIGURE 5. XNOR function optimized lattice structure

This circuit is basically a parallel connection of two series PMOS with another two series NMOS.

The work of the lattice can be explained as follows. If A and B have the same logic state, either one of the parallel connections will connect the output to VDD to get a logic 1. But if they are different, both of the parallel lines are open circuit at either PMOS or NMOS. Hence, XNOR function is achieved.

STEP 2: ADDING PULL-DOWN NETWORKS

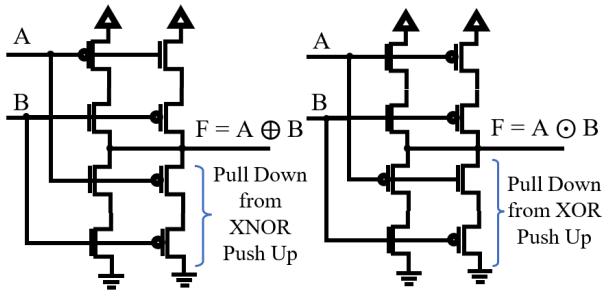
Re-arranging the lattice structure circuits in Figure 4 and 5 to put VDD at the top, and putting resistors as pull-down networks, circuits with better layout as in Figure 6 are obtained.



(a) Resistor pull-down lattice XOR (b) Resistor pull-down lattice XNOR

FIGURE 6. Lattice structure XOR/XNOR functions with resistor pull-down

However, the circuits in Figure 6 are not exactly CMOS compliant because resistors are not ideal pull-down networks and will also draw high current which defeats the earlier objective to reduce power. To solve this, the circuits in Figure 6 need pull-down networks from their inverted functions' push-up networks. Since both of them are complements to each other, they can make use of each other's push-up networks to become pull-down networks in the complementing circuits. These are the finished lattice structure circuits and shown in Figure 7.



(a) CMOS lattice structure XOR (b) CMOS lattice structure XNOR

FIGURE 7. Finished CMOS lattice structure XOR/XNOR gates

SIMILARITY WITH OTHER CMOS XOR GATE

At this point it is worth mentioning that there is a less popular but standard CMOS XNOR gate as shown in Figure 8. This XOR uses only eight transistors and really closely resembles the proposed lattice structure XOR. This is coincidental since anyone with enough experience can deduce the circuit in Figure 8 or Figure 7 simply by experience and observation. However, the step-by-step approach in this paper using lattice structure would generalize the method for any symmetric functions instead of pure observation.

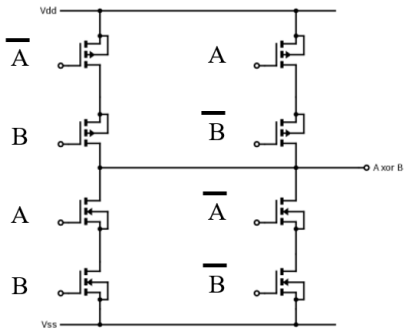


FIGURE 8. A standard CMOS XOR similar to lattice structure result

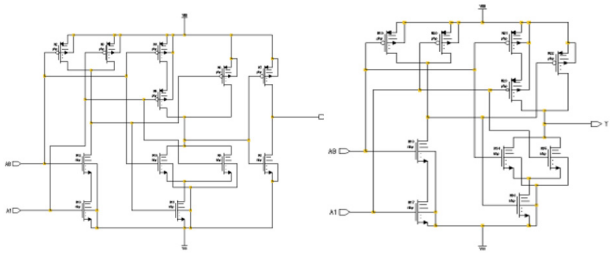
The three key differences between the proposed lattice structure circuit and the circuit in Figure 8 are as follows:

1. All PMOS are located near VDD – as it supposed to be in CMOS – to provide better push-up.
2. All NMOS are located near ground (VSS) – as it supposed to be in CMOS – to provide better pull-down.
3. The circuit requires inverted inputs. If this circuit is to provide these inverters, it requires four more transistors (two transistors for each input). Totaling up to 12 transistors. If the inputs come from registers, the inverted version of the inputs should be easily available and the circuit does not need its own inverters, but this however, requires more complicated wiring.

RESULTS AND ANALYSIS

TRANSISTOR COUNT SAVING

The number of transistors required for the lattice structure XOR/XNOR as given in Figure 7 is eight. The mostly used industry standard XOR and XNOR cell as included in Mentor Graphics comprise of 12 and 10 transistors, respectively. There are two extra transistors in XOR because it consists of an XNOR and an invertor. This means, in terms of transistor count, lattice structure XOR/XNOR have a saving of 33% for XOR and 25% for XNOR.



(a) Industry standard 12-transistor CMOS XOR (b) Industry standard 10-transistor CMOS XNOR

FIGURE 9. Industry standard CMOS XOR/XNOR gates

SIMULATION WAVEFORMS

Simulation of the proposed lattice structure circuit is made on Mentor Graphics 180 nm technology with 1.2 V VDD. The resulting output voltage swing is around 75%: XOR 0.0 V to 0.9 V, XNOR 0.3 V to 1.2 V.

1. XOR logic function is achieved with the following shortcomings (Figure 10):
   a. Logic 1 does not touch VDD as the presence of NMOS in push-up network will introduce voltage drop below VDD.
   b. Logic 0 touches 0 V, but there is a large voltage raise of 0.4 V when both inputs are low (shaded area). The reason for this is because when both inputs are low, the pull-down is made of two series PMOS which is not a good pull-down.
2. XNOR logic function is achieved with the following shortcomings (Figure 11):
   a. Logic 0 does not touch ground as the presence of PMOS in pull-down network will introduce voltage raise above ground.
   b. Logic 1 touches 1.2 V, but there is a large voltage drop of 0.4 V when both inputs are high (shaded areas). The reason for this is because when both inputs are high, the push-up is made of two series NMOS which is not a good push-up.

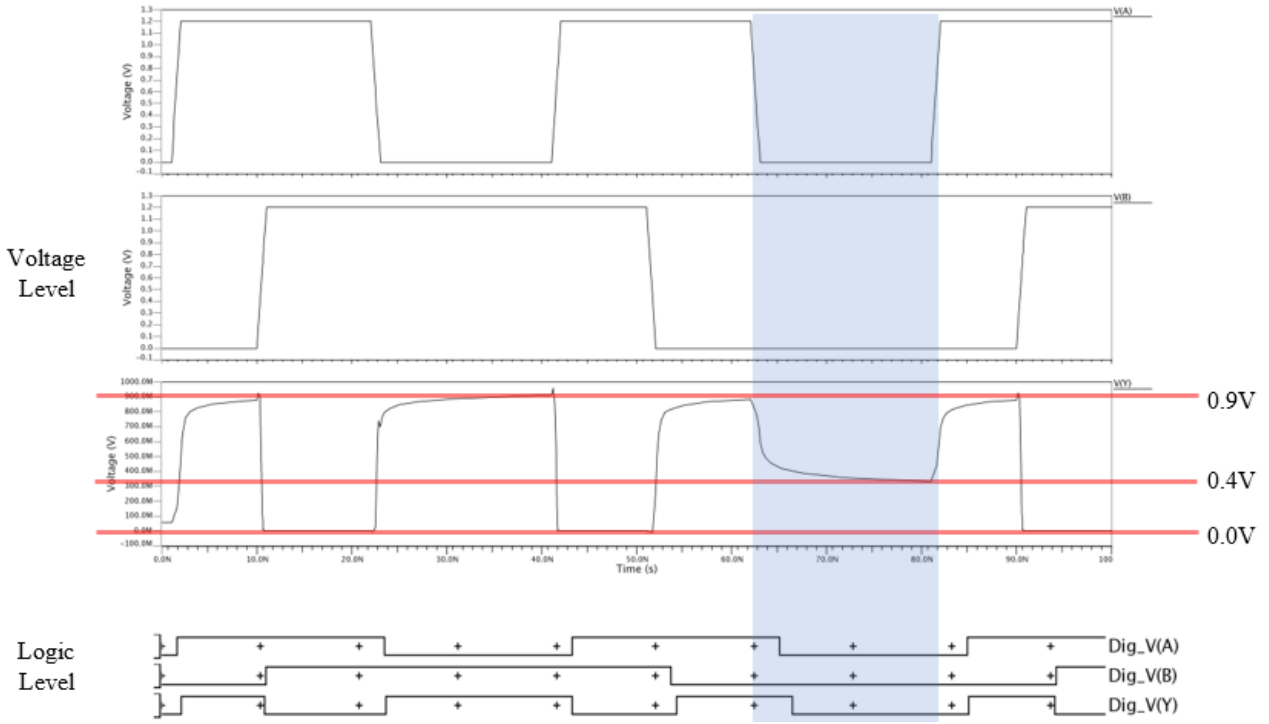


FIGURE 10. Simulation of lattice structure XOR gate

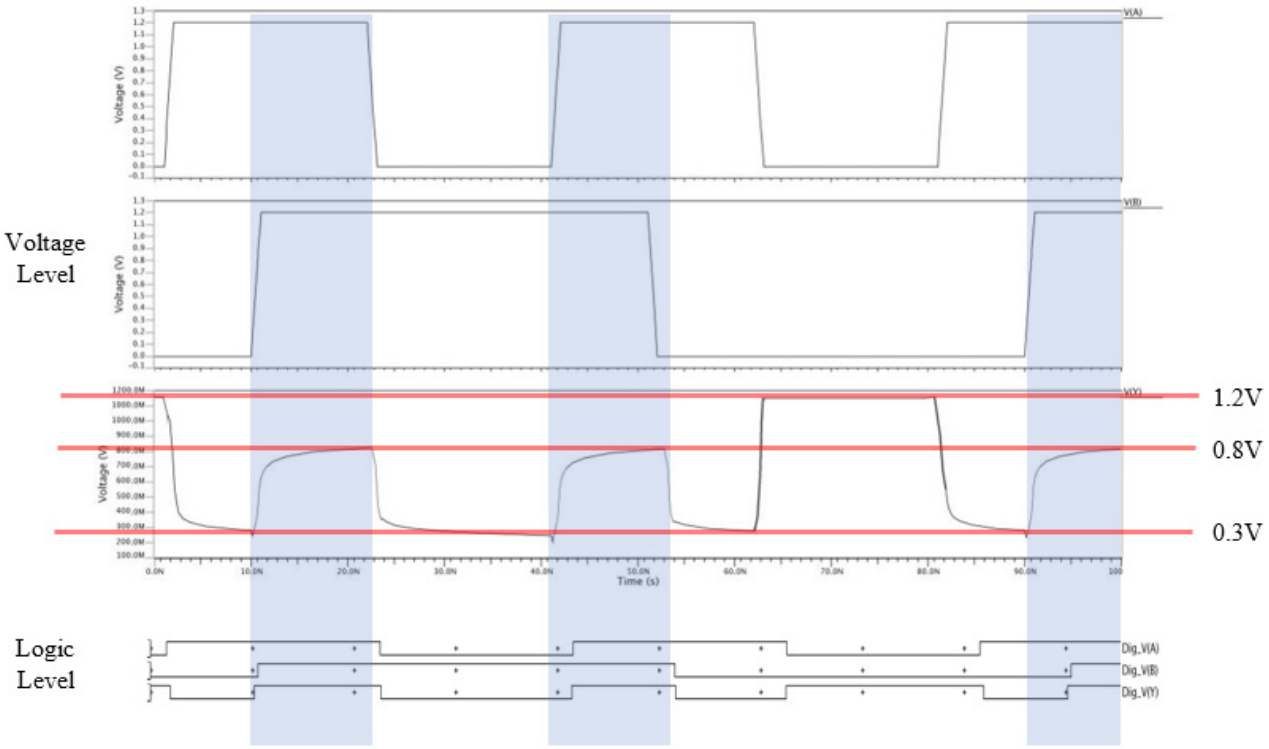


FIGURE 11. Simulation of lattice structure XNOR gate

CONCLUSION

This paper presents a systematic approach to build symmetric function circuits using a classic idea of lattice structure. The attempt is made on XOR and XNOR gates as these two circuits only take two inputs while at the same time prove their significance and usefulness. The functionalities are achieved with the average speed of standard CMOS.

Undoubtedly, there are some issues in the circuits that warrant more work. These include widening the output voltage swing at certain logic combinations. Work on placing PMOS and NMOS at right places is expected to solve this issue by making the circuit to require inverted inputs.

DECLARATION OF COMPETING INTEREST

None

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