

Novel Hybrid Integration of Zeta Converter and Reinforcement Learning for State-of-Charge Balancing Control in an Electric Vehicle Application

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ABSTRACT

State-of-charge (SoC) balancing control is essential in a Battery management system (BMS) of an Electric vehicle (EV) since it aims to maximize the accessible SoC of each cell, which in turn enhances the overall capacity of the battery system. Cell imbalance can have a negative impact on the battery system, without SoC balancing control, some cells might suffer overcharge or deeply discharge than others, affecting the overall performance of an EV. This work presents a comparative study of three emerging DC-DC converters, notably Zeta, SEPIC, and Ćuk converters as well as three controllers namely Proportional integral (PI), Artificial neural network (ANN) and Reinforcement learning (RL) to select the best converter and controller. The comparative study demonstrated that a Zeta converter with an RL controller is the most efficient in terms of output voltage ripple, voltage stress on output voltage, and settling time. A simulation model is developed in MATLAB/Simulink using twenty Lithium-ion battery (Li-ion) cells where this integration intelligently selects active cell combinations to meet the load, aiming to perform rotation among the cells so that they are not overcharged or deeply discharged. A hybrid SoC balancing control incorporating voltage-based using RL controller is designed to perform cell balancing within the battery packs of an EV. The simulation results demonstrated that SoC convergence among twenty Li-ion cells (with SoC difference as little as 0.5 percent) occurs within 10,000 seconds using the proposed hybrid novel integration.

Keywords: Battery management system; electric vehicle; neural network; reinforcement learning; state-of-charge; Zeta converter

INTRODUCTION

Electric vehicles (EVs) are gaining popularity as a means of reducing carbon emissions, conserving fossil resources, and addressing global warming challenges, which have resulted in a paradigm shift away from conventional gasoline and diesel-powered vehicles to EVs. Additionally, EVs offer several advantages over conventional diesel-powered vehicles in terms of reliability, simplicity, and efficiency (Zhang et al. 2021). A Battery management system (BMS) is required to provide an accurate assessment of critical parameters of battery cells, otherwise, the battery system might suffer from severe consequences such as overcharging, deeply-discharging, cell imbalance, and

thermal runaway (Hossain Lipu et al. 2021). Research on monitoring and controlling battery cell conditions in an EV has been carried out extensively where it involves several battery technologies such as nickel-metal hydride, Li-ion, and lead-acid batteries (Ismail et al. 2017; Satyan & Sutar 2020). Extended battery usage and ensuring causality protection remain significant challenges in EV applications. This underscores the importance of individual cell monitoring and State-of-charge (SoC) balancing control within a BMS (Hoque et al. 2016; Naguib et al. 2021).

This paper compares three emerging DC-DC converters i.e., Zeta, SEPIC, and Ćuk, as well as three controllers such as Proportional integral (PI), Artificial

neural network (ANN), and Reinforcement learning (RL) to identify the converter that yields the best performance to be integrated with RL based algorithm. This novel hybrid integration aims to obtain a controllable duty cycle, which is intended to improve the converter's output voltage by eliminating ripples, overshoots, and oscillations in the output voltage as well as to perform SoC balancing control among twenty Li-ion cells. A simulation model is developed in MATLAB/Simulink to demonstrate the effectiveness of the proposed integration. This paper is organized as follows: Firstly, discusses several active cell balancing techniques focusing on those that employ DC-DC converters. Secondly, presents the comparative analysis of the performance of three emerging DC-DC converters i.e., Zeta, SEPIC, and Cuk converters. Thirdly, presents the comparative analysis of the performance of three controllers such as PI, ANN, and RL to suggest the most suitable control technique for SoC balancing application in an EV. And, following the proposed hybrid integration for SoC balancing control as well as simulation results. The conclusion is presented at the end.

SOC BALANCING CONTROL TOPOLOGIES USING DC-DC CONVERTERS

Active cell balancing is preferred over passive cell balancing, particularly in applications where maximizing available capacity is crucial (Ahmad et al. 2019). Active cell balancing utilizes inductive or capacitive charge shuttling mechanisms to transfer charge from a highly charged cell to a less charged cell, aiming to eliminate cell imbalance.

Active cell balancing compensates irregularities such as capacity, internal resistance, and random degradation of cells by shifting electrical energy from cells with higher SoC to cells with lower SoC (Omariba et al. 2019). Figure 1 depicts active cell balancing topologies. Several works have been conducted to perform active cell balancing using a DC-DC converter (Sugumaran & Amutha Prabha, 2023; Arzu et al. 2020; Ceylan & Abdulkadir Balikci 2023). to perform bi-directional power transfer between battery packs and the load to achieve SoC convergence among battery cells during charging and discharging.

In (Galvão et al. 2022) a novel method of charge equalization is introduced for series-connected battery cells. This technique employs a multi-winding transformer, and an isolated DC-DC converter equipped with a capacitive output filter. The proposed scheme applies to both flyback and forward converter topologies. During the charging process, initiated at a low level of charge, the

highest current that the charger can provide to the battery pack is delivered. As the SoC increases, the charging current is gradually reduced. Additionally, the algorithm incorporates rest periods, aimed at mitigating temperature differentials between colder and warmer cells. Equalization charging is employed to enhance battery capacity at lower current levels. Importantly, this approach offers cost-effective implementation and contributes to prolonging the battery cell's lifespan.

In (Samanta & Chowdhuri 2021), a method utilizing a dual DC-DC converter is introduced. This approach employs a flyback converter to facilitate pack-to-cell balancing during pack charging. Conversely, during the discharging phase, a buck converter topology is employed for balancing the auxiliary lead-acid battery with the Li-ion battery cells. Additionally, energy generated from regenerative braking is harnessed to expedite cell balancing within an EV and enhance the efficiency of the balancing process. The highlight of this work is the use of auxiliary batteries to perform balancing, which results in the reduction of the number of active components, power switches, and control complexity.

A two-stage charge balancing scheme with the optimal power rating design rule is proposed for series-connected Li-ion cells in hybrid EVs by employing conventional low-power and minimized flyback converters (Ahmad et al. 2023). They are intra-module and inter-module charge balancing approaches. In intra-module charge balancing, the primary sides of flyback converters are parallelly connected for charging selected cells within the module. Flyback converters are employed for inter-module charge balancing with secondary windings electrically connected in parallel for automatic charge balancing among the modules in the hybrid EVs. The current-fed type charge balancing scheme within the module and the voltage-fed type charge balancing scheme among the modules have not only achieved SoC convergence for a sample of forty cells but also allowed low voltage stress on all the power semiconductor devices in the proposed circuit configuration.

An active charge equalization method employing a buck converter is proposed in (Sugumaran & Amutha Prabha 2023), where it can achieve SoC balancing among idling cells, in addition to during charging and discharging. This feature is especially significant to EV applications since the battery cells of an EV stay idle for a long period compared to battery cells in other applications such as power grids. SoC balancing among idling cells could maximises the available energy of the battery pack as well as and reliability of stack operation in the long run. Figure 1 depicts existing active cell balancing topologies, which can be distinguished into two major categories, i.e., non-converter-based and converter-based.

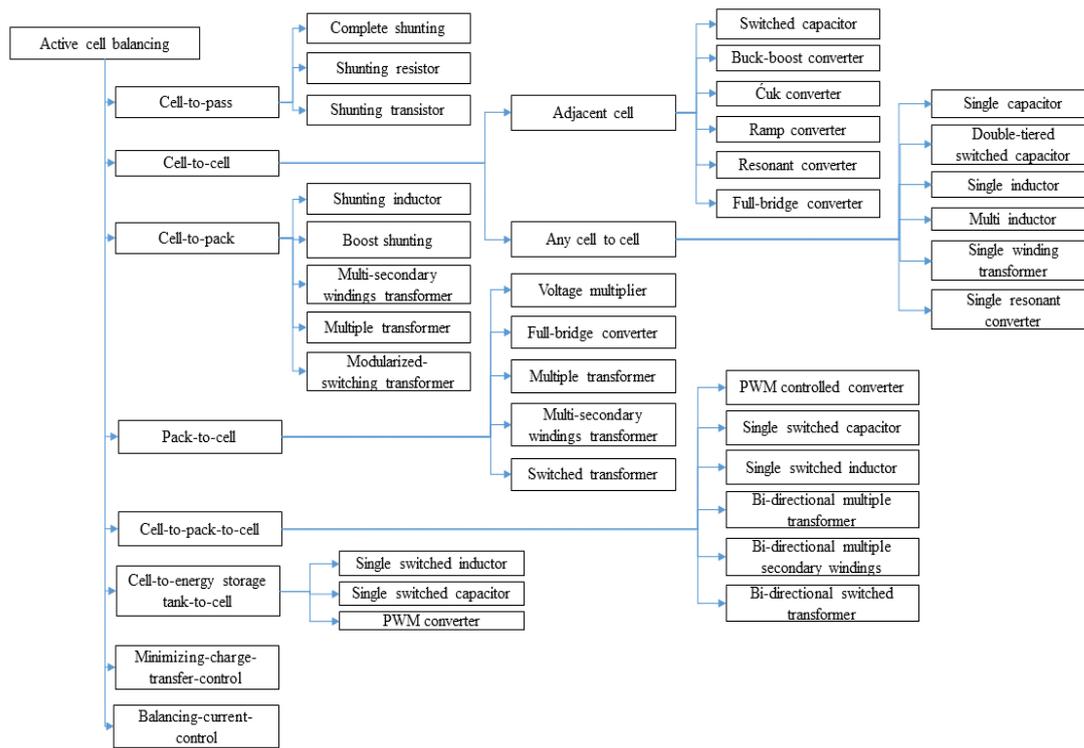


FIGURE 1. Active cell balancing topologies (Khan, Chia Ai Ooi, Abdulrahman Alturki, et al. 2024; Venugopal et al. 2023).

When selecting an optimal DC-DC converter topology, factors such as the number of components, power rating, conversion efficiency, voltage stress, peak overshoot, and voltage conversion ratio must be taken into account. The number of circuit components significantly affects system complexity, directly influencing both the size and cost. The primary goal of balancing control is to eliminate inconsistencies in capacity, internal resistance, and/or random degradation in battery cells with the least amount of balancing time and power loss possible. It is worth noting that the efficiency of a DC-DC converter would significantly affect the performance of the balancing control implemented on the Battery energy storage system (BESS) of an EV. The parameters of the converters, such as duty cycle and switching frequency, on the other hand, are directly related to the balancing control system performance indicators, such as convergence speed and stability. The balancing control adjusts the converters' parameters to achieve the SoC convergence. With this regard, the advantages, and disadvantages of three commonly used non-isolated converters, i.e., Zeta, SEPIC, and \dot{C} uk converters are

presented in Table 1. The advantages and disadvantages of Zeta, SEPIC, and \dot{C} uk converters are presented to identify the best converter to be integrated with ANN, which is described below.

COMPARATIVE ANALYSIS OF THE PERFORMANCE OF THREE EMERGING DC-DC CONVERTERS

Before the implementation of the proposed integration, the performance of three emerging DC-DC converters, i.e. Zeta, SEPIC, and \dot{C} uk converters in the context of EV are studied and evaluated via simulation model in MATLAB/Simulink, aiming to select the best converter among three to be used in the proposed integration. The simulation parameters shown in Table 2 are applied to all three converters for fair comparison. The performance of these three converters is compared in five categories, i.e. ripple voltage, settling time, output voltage stress, overshoot, and efficiency as shown in Table 3.

TABLE 1. Advantages and disadvantages Of Zeta, Sepic, and Ćuk Converters (Promphak Boonraksa et al. 2021; G. Sree Lakshmi & S. Naveen Kumar, 2023; Parthasarathy et al. 2016; Manikandan et al. 2020; Kushwaha et al. 2020; turksoy et al. 2020)

DC-DC converter	Advantages	Disadvantages
Cuk	Modular design and easy control Provide output voltage with opposite polarity of the input Can be used for both current and voltage control	High complexity Voltage polarity is inverted and difficult to stabilize
SEPIC	Deliver output voltage maintaining the same polarity as the input voltage. Very low current and voltage ripple at the input side	High control High complexity Very high current and voltage ripple at the output side Slow settling time Voltage polarity is inverted and difficult to stabilize
Zeta	Simple design Output voltage is non-inverted Ripple free output current Fast settling time and low switching stress	Relatively very high current and voltage ripple at the input side High control complexity High voltage stress

TABLE 2. Simulation Parameters

Parameters	Value
Input voltage	400 V
Switching frequency	50 kHz
Duty cycle	0.5556 %
Output voltage	500 V
L_1	1 mH
L_2	1 mH
C_1	10
C_2	10

TABLE 3. Performance of Zeta, Sepic, and Ćuk Converters

Parameters	Zeta	SEPIC	Ćuk
Ripple voltage (V)	0.1	0.68	0.1
Settling time (s)	0.03	0.08	0.04
Voltage stress (V)	902	903.5	903.5
Overshoot	415	376	420
Efficiency (%)	86.39	85.10	85.75

RIPPLE VOLTAGE

The output ripple voltage of the Zeta and Ćuk converters is very low (0.1 V) compared to that of the SEPIC converter due to the existence of a series inductor and LC low pass filter with output voltage in both the converters. The inductor prevents rapid change in output current, thus reducing the ripples in output voltage. A higher value of inductance results in a lower ripple. On the other hand, a larger inductor comes with higher resistance, which reduces the efficiency of a DC-DC converter. To overcome this, a suitable inductance value that is just sufficient to keep the voltage and current ripple under acceptable range should be chosen in a converter (Karuppiyah et al. 2020). The ripple

of output voltage and current of the SEPIC converter is extremely high which can be observed in Figs. 2(a) and (b). Excessive power losses and distortion caused by increased output voltage ripple in a DC-DC converter could significantly affect the performance of battery cells in an EV as it causes premature aging of the battery cells, which further reduces the available capacity of the battery cells in the long run.

SETTLING TIME

Zeta, SEPIC, and Ćuk converters are sophisticated fourth-order circuits featuring both real and complex poles and

zeros. As the circuit's order increases, output fluctuations and power loss become more prominent. To address this challenge, the pole-zero cancellation method is used, which eliminates poles and zeros from the transfer function, thereby reducing the system's order and minimizing these adverse effects. Consequently, the non-existence of zeros in the right half-plane of a Zeta converter results in a lower settling time (0.03 ms) compared to Ćuk (0.04 ms) and SEPIC (0.08 ms) converters respectively. A DC-DC converter with a lower settling time is preferred in EV applications to mitigate power losses and to guarantee a constant output voltage which benefits more in the aspect of SoC balancing control among the battery cells in an EV (Shabbir et al. 2016).

VOLTAGE STRESS

When the energy stored in an inductor or capacitor of a DC-DC converter is released, occasionally it might result in high voltage stress in the power semiconductor devices

in the DC-DC converter. A DC-DC converter's efficiency is further diminished by increased conduction losses resulting from high voltage stress. As Table 3 shows, the Zeta converter has demonstrated the least voltage stress when compared to the SEPIC and Ćuk converters.

EFFICIENCY

The factors discussed above affect the performance as well as the efficiency of a DC-DC converter. From the simulation result presented in Table 3, the Zeta converter has the lowest voltage stress, the lowest settling time, and the lowest ripple voltage. As a result, the Zeta converter yields a higher efficiency compared to the other two converters. Therefore, the Zeta converter is chosen as the candidate for the proposed hybrid integration explained below. An efficient DC-DC converter is essential in the proposed integration as converter control is used to intelligently select battery cells to be charged or discharged to achieve SoC balancing for the battery bank in an EV.

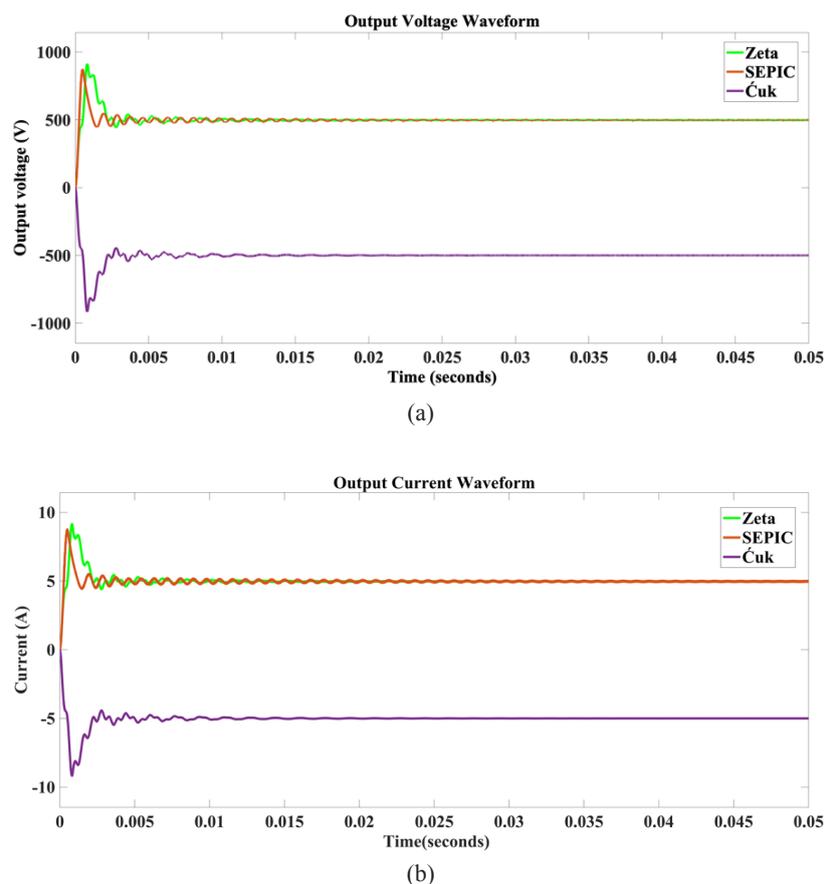


FIGURE 2. Waveforms of Zeta, SEPIC, and Ćuk converters for (a) output voltage, and (b) output current.

COMPARATIVE ANALYSIS OF THE PERFORMANCE OF THREE CONTROLLERS PI, ANN, AND RL

Because of their switching behavior, DC-DC converters exhibit nonlinearity and demonstrate moderately damped dynamics (Radwan & Azad, 2022). Thus, it is imperative to utilize an appropriate control method for DC-DC converters to attain a stable and regulated output voltage. While conventional linear regulators like PI regulators can be used for control, they tend to perform inadequately under heavy loads and when system parameters vary (Huang et al. 2019). Intelligent controllers like ANN are utilized to tackle these challenges due to their rapid response, exceptional dynamic performance, and robust control capabilities. However, the use of ANNs leads to an increased controller size due to the need for significant training data and additional computational requirements.

PI CONTROLLER

The PI controller can be employed to enhance stability and mitigate significant disturbances during system operation due to its zero-control error and resistance to measurement channel variations (Anushree Ramanath, 2024). The PI controller calculates the error value continuously as the difference between the desired value and the measured value and then applies a correction based on proportional and integral terms. The letter “P” in the PI controller is proportional to the current error value, if the error is large, applying the gain factor K_p will also make the regulated output large. When relying on proportional controls, there is still a difference between the desired and measured values. As a result, integral controllers with proportionality are utilized to minimize the proportional impact and boost system accuracy. Using the gain factor K_i , the integral element, the term “I,” accounts for prior values of error and integrates them over time.

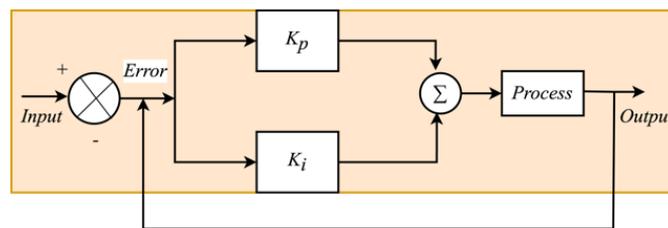


FIGURE 3. Illustration of PI controller.

ANN CONTROLLER

To improve the dynamic response of the Zeta converter, ANN is used due to its capability of finding complex non-

linear relationships between dependent and independent variables without an accurate mathematical model of the system (Kumar et al. 2024).

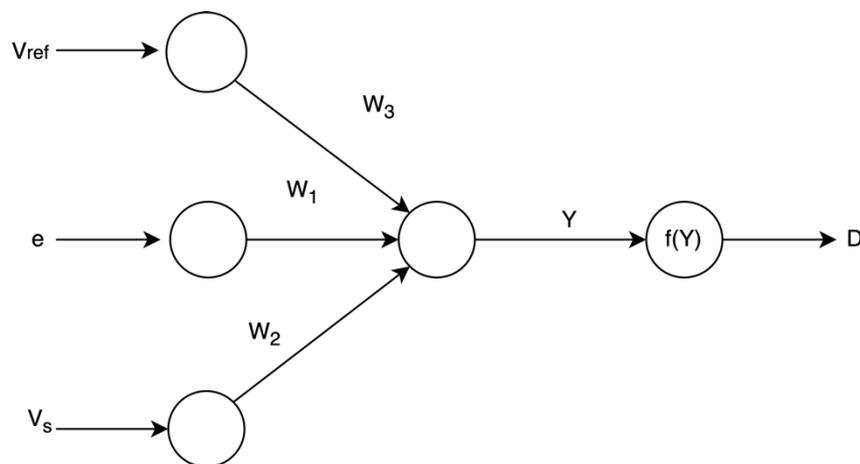


FIGURE 4. ANN consists of three layers.

In this work, a feed-forward neural network is used as depicted in Figure 4. The term “feed-forward” implies that information from the input layer is propagated to the output layer without a feedback phase. The ANN consists of three layers with an input layer consisting of three neurons, i.e. reference voltage, error, and Zeta output voltage. Error is defined as the difference between reference voltage and Zeta output voltage. W_1 , W_2 , and W_3 are the connection weight parameters between the neurons. The output layer yields the duty cycle. The trained network is used to produce the required output, which is the duty cycle in response to three inputs, allowing us to see how closely the actual outputs match the desired ones. The duty cycle obtained from ANN varies as the reference voltage changes. ANN aims to reduce the error by adjusting the duty cycle to obtain the desired Zeta output voltage, which is as close to the reference voltage as possible.

In this work, data (input and output data) is collected from the previous PI controller for the training of ANN. The ANN updates the weights (W_1 , W_2 , and W_3) according to the input and output data to depict the accurate duty cycle. In Figure 6(b), it can be observed that the duty cycles change as the reference voltage changes.

RL CONTROLLER

A type of machine learning called RL involves an agent interacting with its surroundings and changing its behavior in response to rewards. RL aims to teach an agent to perform a task in an unfamiliar environment. The environment supplies the agent with observations and a reward, prompting the agent to respond by taking action. The reward reflects the effectiveness of an action in achieving its goal. Here the environment is the Zeta converter to be controlled by the RL agent by predicting the appropriate duty cycle to provide the desired output voltage of the Zeta converter by collecting the maximum reward from the environment. The number of episodes is taken as 30 and the average reward is set to 240. MATLAB/Simulink RL toolbox is used to create the DQN (Deep Q-network) agent. Figure 5 depicts the episode-by-episode reward. Once the average reward reaches 240, the training process for the agent is terminated. Table 4 outlines the hyperparameters employed in the algorithm.

TABLE 4. Hyperparameters used in DQN Algorithm

Hyperparameters	Value
Sample time (s)	0.1
Experience buffer length	10^6
Target smooth factor	10^{-3}
Learning rate	0.01
Mini batch size	64
Maximum episode length	20

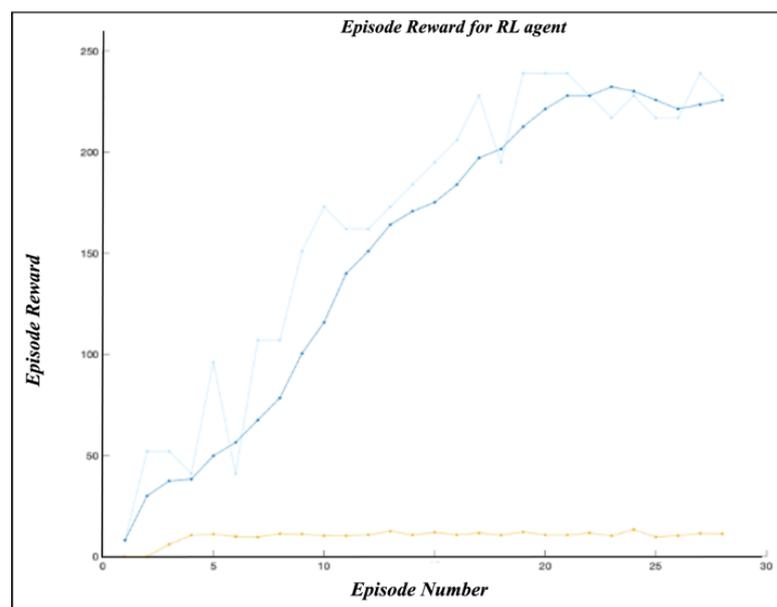


FIGURE 5. Episode reward for RL controller.

A Zeta converter is developed in MATLAB/Simulink with an input voltage of 3.6V. The reference voltage is initially taken to be 3.5V, then after a specific amount of time (1sec), it is increased to 4.44V. The simulation parameters shown in Table 5 are applied to all three

controllers for fair comparison. The performance of these three controllers is compared in five categories, i.e., ripple voltage, settling time, rise time, overshoot, and efficiency by changing the reference voltage of the Zeta converter as shown in Table 3.

TABLE 5. Simulation Parameters

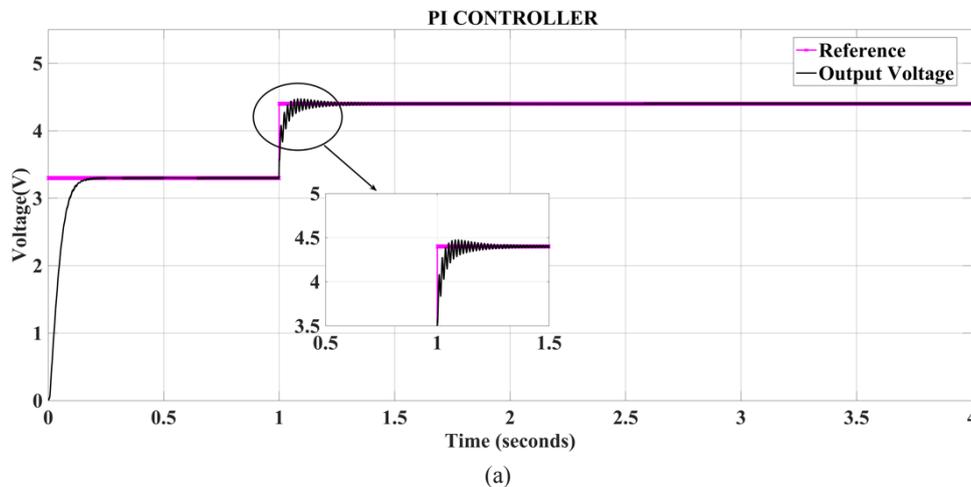
Parameters	Value
Input voltage	3.6 V
Switching frequency	25 kHz
Reference voltage	3.5 V & 4.44 V
C_1	720
C_2	15
L_1	1.6 mH
L_2	1.6 mH

TABLE 6. Performance of PI, ANN, and RL Controllers

Parameters	PI	ANN	RL
Ripple voltage (V)	0.06	0.01	0.05
Settling time (s)	0.25	1	0.125
Rise time (s)	0.25	0	0.001
Peak Overshoot (%)	0.068	0.081	0.092
Efficiency (%)	85.39	86.10	86.75

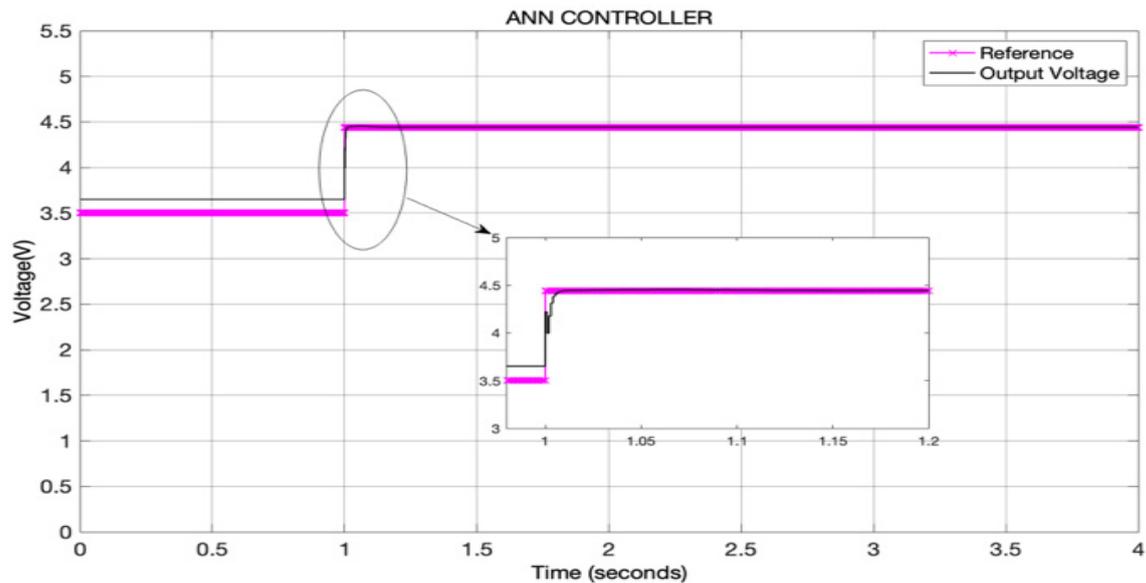
Figs. 6(a), 6(b), and 6(c) represent the output and reference voltages with the PI controller, ANN controller, and RL controller and it shows that the PI and RL controller track the reference voltage accurately. However, the ANN controller does not converge to the initial reference voltage (3.5V). Whereas the output ripple voltage of the ANN controller (0.01 V) is less as compared to the PI (0.06V) and RL (0.05V) controller. Moreover, the peak overshoot of PI (0.068%) and ANN controller (0.081) is comparatively low as compared to the RL (0.092) controller. Additionally, the settling time and rise time of the RL controller are very low as compared to the other two controllers namely the

PI and ANN controllers. The factors discussed above affect the performance as well as the efficiency of the controllers. From the simulation result presented in Table 6, the RL controller has the lowest rise time, settling time, and ripple voltage. As a result, the RL controller yields a higher efficiency compared to the other two controllers i.e., PI and ANN. Therefore, RL controller is chosen as the best controller for the proposed hybrid integration explained in Section V. An efficient RL controller is essential in the proposed integration as converter control is used to intelligently select battery cells to be charged or discharged to achieve SoC balancing for the battery bank in an EV.

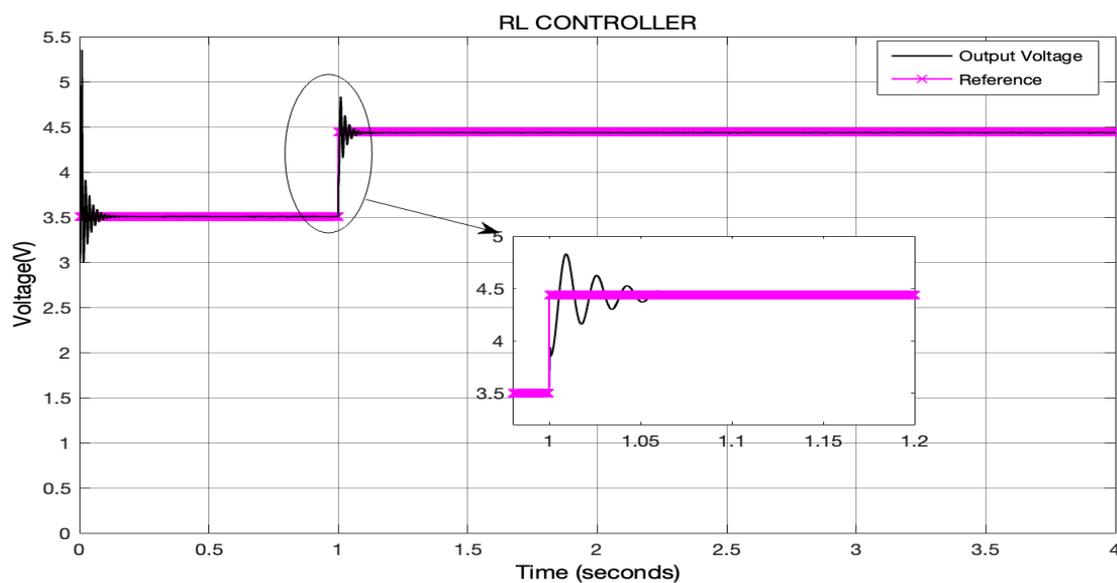


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(b)



(c)

FIGURE 6. Output voltage Waveforms of (a) PI, (b) ANN, and (c) RL controllers.

PROPOSED INTEGRATION OF ZETA CONVERTER AND REINFORCEMENT LEARNING

Simulation work has been performed in MATLAB/Simulink to investigate the effectiveness of SoC balancing control among twenty battery cells using the proposed integration of the Zeta converter and RL algorithm. In Figure 7, a novel hybrid energy management system incorporating a Zeta converter and RL is proposed to perform SoC balancing control among battery cells in an

EV. The zeta converter is employed to provide bi-directional power transfer between the source and load of the converter while RL is applied to the Zeta converter to achieve a controllable duty cycle of the power semiconductor devices in the Zeta converter.

Several AI algorithms have been developed to improve the dynamic response of DC-DC converters (Wang et al. 2023; Ram et al. 2021) where the AI controllers aim to optimize the output voltage and dynamic response of DC-DC converters (Ramirez-Hernandez et al. 2019). RL is one of these intelligent controllers and it has been widely implemented in applications such as harmonic detection

and elimination, robotics, aerospace, automotive, telecommunications, medical, and photovoltaic systems (Ramirez-Hernandez et al. 2019). The benefit of employing RL is that it learns from experience even in the absence of a training dataset (Bianchi et al. 2016). In this work, a DQN-based RL controller with a Zeta converter is used and depicted in Figure 7. The DQN-based RL controller consists of a neural network (NN) that contains 3 layers namely the input layer, output layer, and hidden layer. Hidden layer consisting of 256 neurons. RL agent has three inputs as observations, reward, and IsDone and generates output as action (duty cycle). Error and integrated error are taken as observations. Error is typically defined as the disparity between the reference voltage and the output voltage of the Zeta converter.

IsDone is True if the converter output voltage is greater than 8V. A reward function is defined in Eq. 1 below:

$$Reward = \begin{cases} 10 & \text{if error} \leq 0.1 \\ -1 & \text{if error} > 0.1 \\ -20 & \text{if IsDone} = True \end{cases} \quad (1)$$

The trained network is used to produce the required output, which is the duty cycle in response to three inputs, allowing us to see how closely the actual outputs match the desired ones. The duty cycle obtained from RL varies as the reference voltage changes. The difference between the desired duty cycle and the RL output is referred to as an error, and RL aims to reduce the error by adjusting the duty cycle to obtain the desired Zeta output voltage, which is as close to the reference voltage as possible. In Figure 6(c), it can be observed that the duty cycles obtained for the reference voltage of 3.5 V and 4.4 V are 55 % and 60 %, respectively.

In a Li-ion battery pack, three approaches to SoC balancing are commonly used: voltage-based, capacity-based, and SoC-based. The most common indicators for cell inconsistencies are cell voltage and SoC. While SoC cannot be directly measured, it can be estimated based on various cell parameters such as internal resistance, open circuit voltage (OCV), temperature, charging, and discharging current. Voltage-based SoC balancing approach is reliable and efficient and is frequently employed in existing works for EV applications (Khan et al. 2024; Kishore et al. 2022).

In this work, a voltage-based algorithm for SoC balancing is implemented as demonstrated in Figure 8. Firstly, the cell voltage of each cell is checked to see if they are within 0.02 V of each other. If this is not the case,

balancing control has to take place, which begins by calculating the average voltage (V_{avg}) of all twenty cells based on Eq. 2. Each cell voltage is compared to V_{avg} , if it is greater than V_{avg} , the cell is connected to the input side of the Zeta converter, indicated by MOSFET switches ($s_{1i}, s_{2i}, \dots, s_{(n-1)i}, s_{(n)i}$) in Figure 6. Whereas the cells with voltage less than or equal to average voltage, are connected to the output side of Zeta converter, indicated by MOSFET switches ($s_{1o}, s_{2o}, \dots, s_{(n-1)o}, s_{(n)o}$) in Figure 7. Once the cells with maximum and minimum voltage are placed accordingly in the converter, the duty cycle generated from RL is used to generate the pulse width modulation (PWM) signal to each MOSFET of the Zeta converter. Energy is transferred from the cell at the input side of the converter (with higher energy) to the output side of the converter (with lower energy) until the cells reach a voltage that is within 0.02 V from the average voltage.

$$V_{avg} = \frac{(V_1 + V_2 + V_3 + \dots + V_n)}{n} \quad (2)$$

where V_1, \dots, V_n represent the voltage of cells $1, 2, \dots, n$. n is the total number of cells. Table 4 depicts the simulation parameter values used in this work. SoC balancing control is performed to balance twenty Li-ion battery cells. In Figure 9, the initial SoC for all cells is set to range between 61.1 % to 77.7 %. It can be observed that the balancing process starts by having cells with higher energy discharging to cells with lower energy. Cells with the highest voltage indicated by V_{max1} and cells with the lowest voltage indicated by V_{min1} are selected. These two cells are connected to the input and output of the converter, respectively. Energy is transferred from the cell indicated by V_{max1} to the cell with V_{min1} . Consequently, the SoC for the cell with V_{max1} decreases while the SoC for the cell with V_{min1} increases. When the cell (V_{min1}) reaches V_{avg} at $t=1800$ s, the corresponding switches of the cell (V_{min1}) are turned OFF, and the corresponding switches of the next lowest cell (V_{min2}) are turned ON. The cell is connected to the converter's output side and is charged by the (V_{max1}) cell. It can be observed that the cell (V_{max1}) reaches V_{avg} at $t=1800$ s. As a result, the corresponding switches in cell (V_{max1}) are turned OFF, while the corresponding switches in cell (V_{max2}) are switched ON. The balancing process continues until around $t = 9700$ s all twenty cells are balanced with the cell voltage difference less than or equal to 0.02 V. The SoC difference has now reduced from 16.6 % (when $t = 0$ s) to 0.5 % (when at $t = 9700$ s).

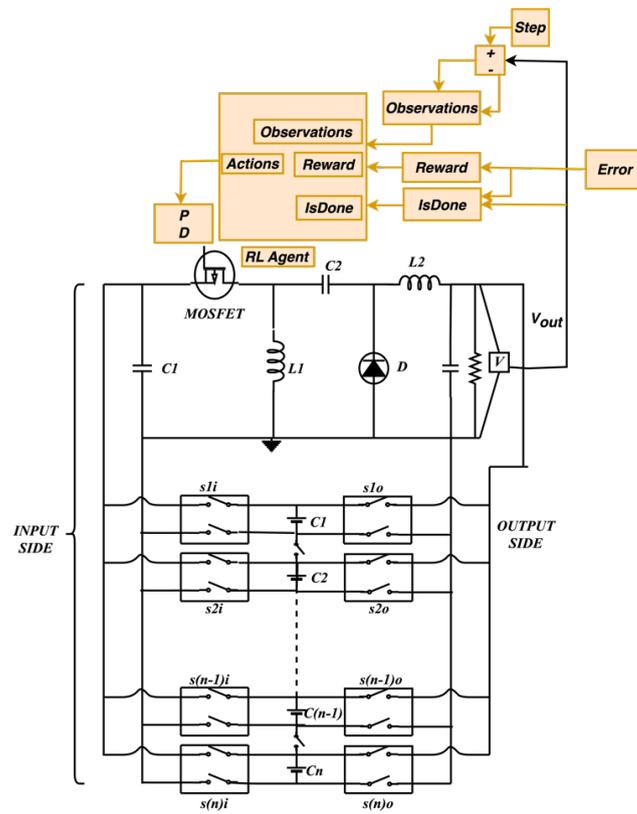


FIGURE 7. The proposed integration of Zeta converter and RL.

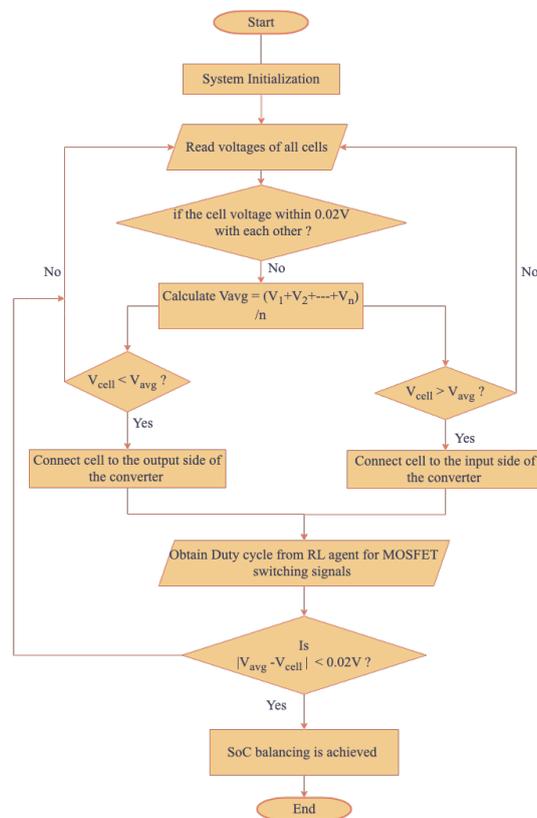


FIGURE 8. Flowchart of cell selection based on duty cycle control by RL.

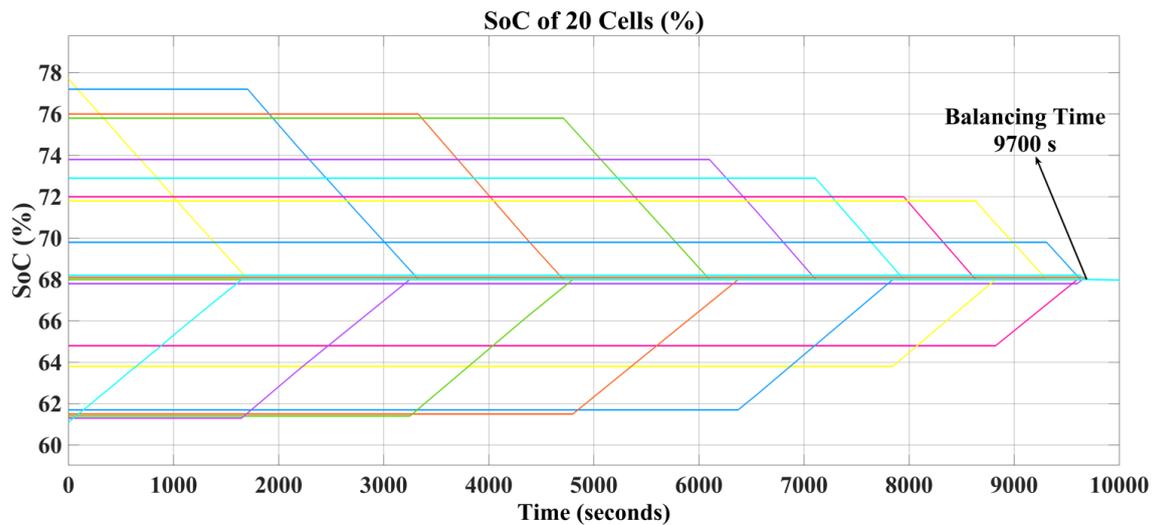


FIGURE 9. SoC balancing control for a battery pack of twenty cells using the proposed integration.

CONCLUSION

The proposed integration of the Zeta converter and RL has been validated in MATLAB/Simulink where it has been shown to achieve SoC convergence among twenty Li-ion cells within 10,000 s. Before this work, a comparative analysis was performed among Zeta, SEPIC, and Ćuk converters and it demonstrated that the Zeta converter is the most efficient in terms of output voltage ripple, voltage stress on output voltage, and settling time compared to SEPIC and Ćuk converters. Moreover, a comparative analysis is performed among PI, ANN, and RL controllers and it demonstrated RL controller-based Zeta converter is more efficient in terms of settling time and rise time as compared to PI and ANN controllers. With the hybrid SoC balancing control incorporating voltage-based and RL-based algorithms, this integration intelligently selects active cell combinations to meet the reference voltage, which enables cell rotation with charge transferred from cells with higher energy to the cells with lower energy within the battery packs of an EV.

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DECLARATION OF COMPETING INTEREST

None.

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